Development and Testing of an TDC-based data and timing transfer scheme for the CLICK mission

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Presentation Overview

CLICK: CubeSat Laser Infrared CrosslinK

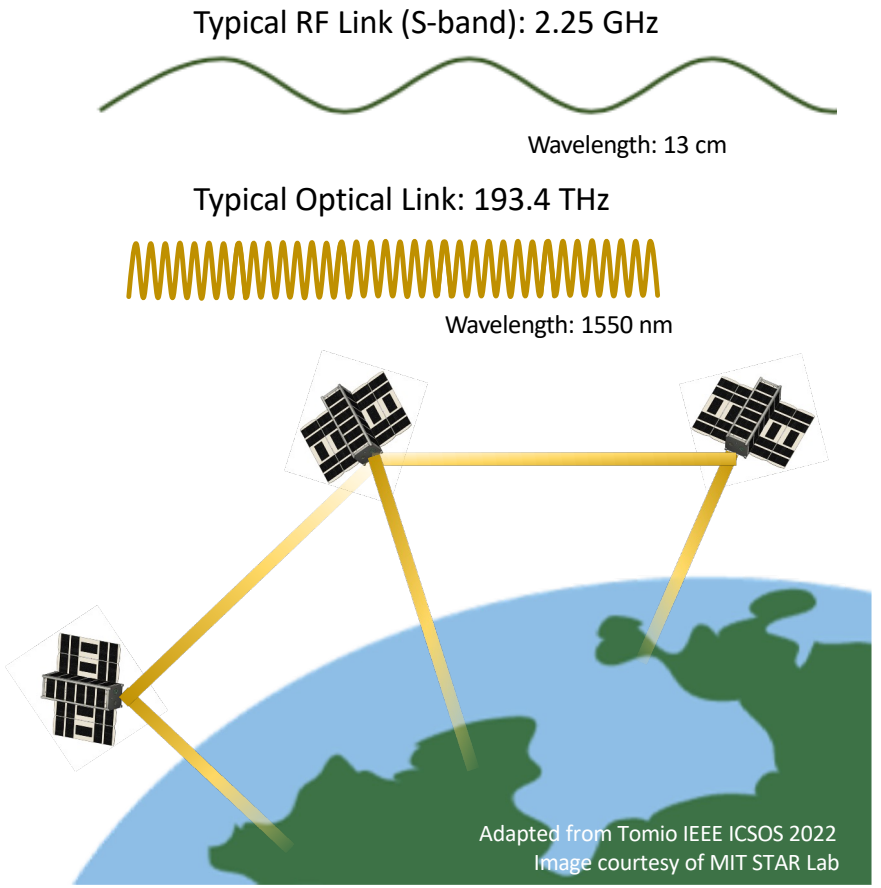
- CLICK Mission and Motivation
  - CLICK A and CLICK B/C
- TDC Receiver (RX) & Transmitter (TX) for transfer scheme
- Flatsat testing in electric loopback mode
- Future work

CLICK Motivation

- Tech demo for laser crosslink with low SWaP
  (Seize, Weight and Power)

- Why laser com? VS (RF):
  - Higher optical frequency
  - Higher modulation rates
  - Less divergence (power, security)

- Future/present constellations:
  - Gbps-rate full-duplex crosslinks
  - Precision ranging and timing



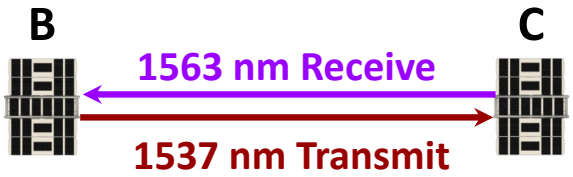
CLICK Mission

Mission Goal: Demonstration *of* ***low-SWaP, full-duplex, high data rate laser communication,*** *timing transfer and ranging between two (3U)* ***CubeSats using COTS (commercial off-the-shelf) components***

CLICK A

- Operations: Sept. 2022 – Mar. 2023
- Single 1.2 U, 1.2 kg, <15 W payload
- Risk-reduction mission
- Successfully tested:
  - MEMS Fast Steering Mirror and PAT capabilities
  - Pointing error data
  - Spacecraft bus hardware and software, ground support systems, optical ground station

CLICK B/C



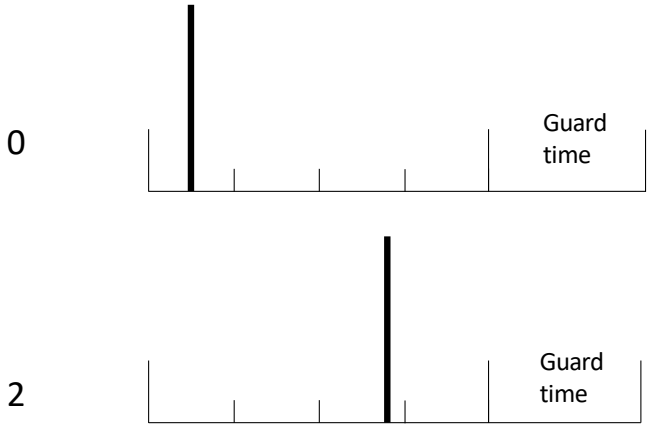
- Crosslink and downlink
- Pair of 1.5 U, 1.5 kg, <30 W payloads

Launch to ISS: Early 2025

CLICK-B/C data transfer

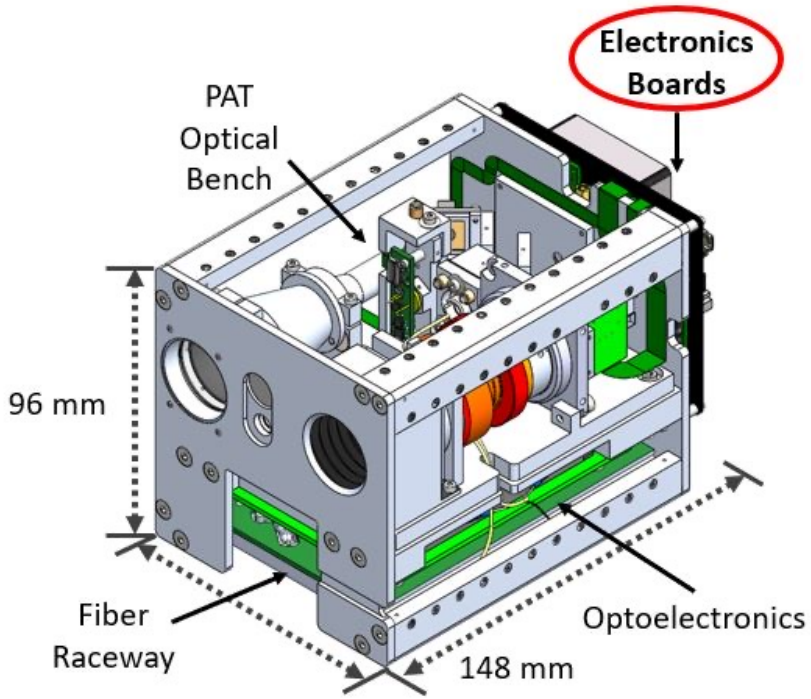
- Full-duplex Pulse Position Modulation (PPM) crosslinks (1537/1565 nm)
  - 50 Mbps, 4-PPM
  - 25 Mbps, 16-PPM
  - 25-580 km range
- Timing error from slot deviation:
  - 200 ps timing accuracy

4-PPM (# of slots here) – encoding 2bit words



CLICK-B/C Payload

- Optical bench, fiber raceway and electronic boards in 1.5 U

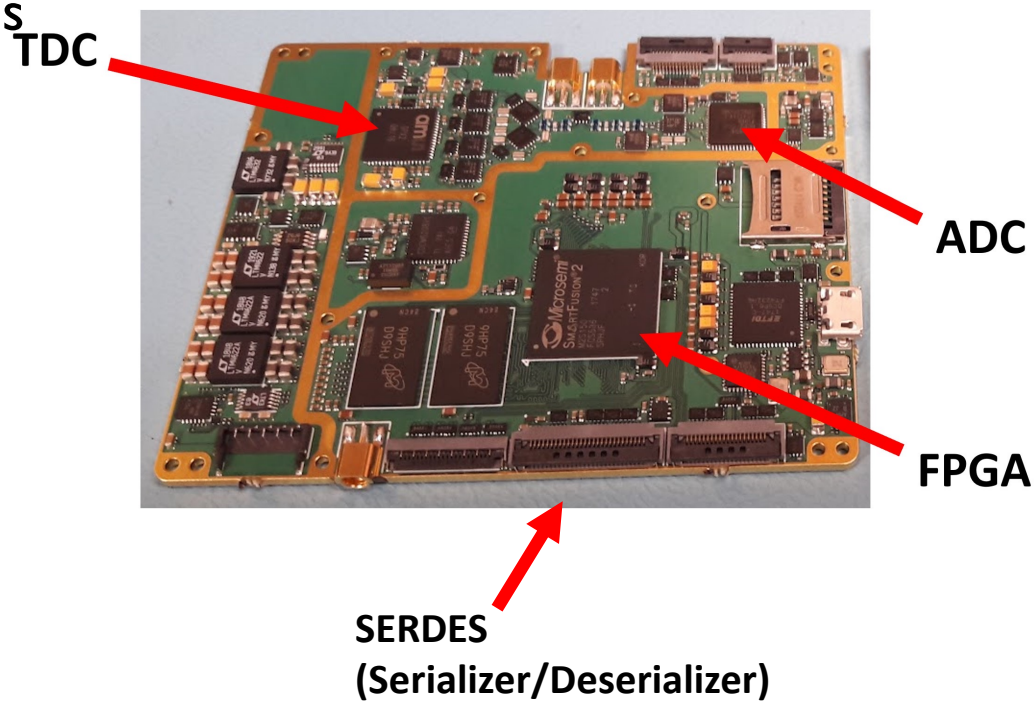


Tomio, 2022. ICSO.

TDC Chain Hardware

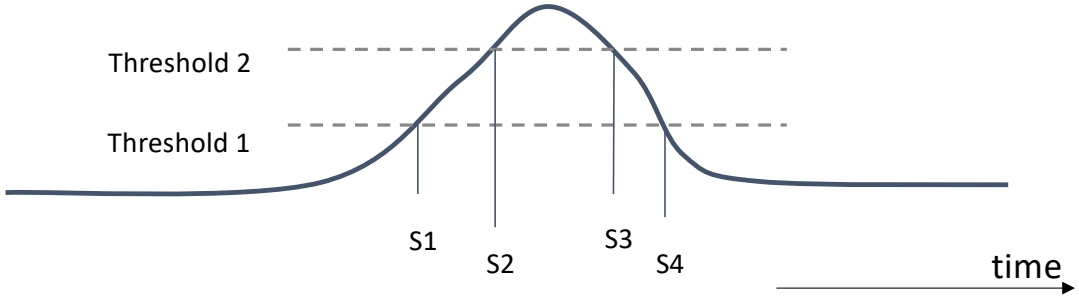
- 4 channel Time-to-Digital converter (TDC) timestamps pulses at 4 times
- FPGA averages into single timestamp per pulse
- FPGA hosts PPM decoder
- TX pulses are generated on the FPGA and transmitted via SERDES
- (Parallel ADC receiver chain)

FPGA Board

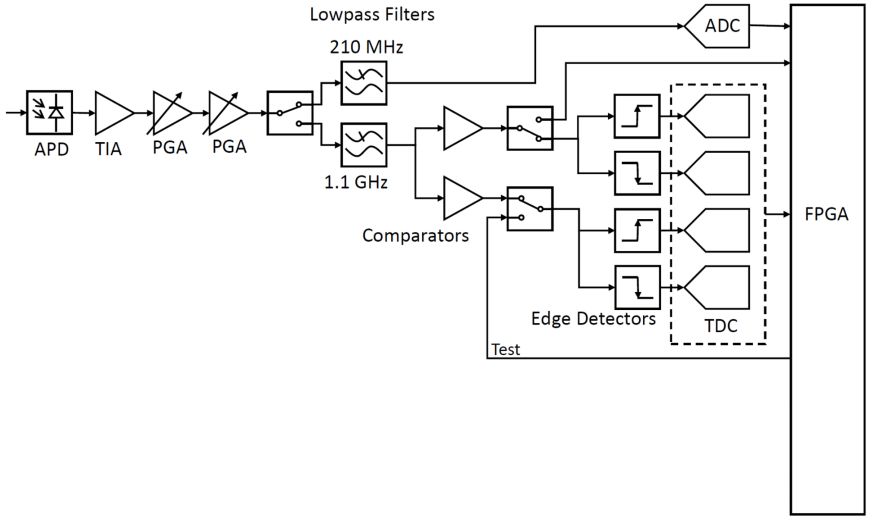


TDC Receiver: Front-end

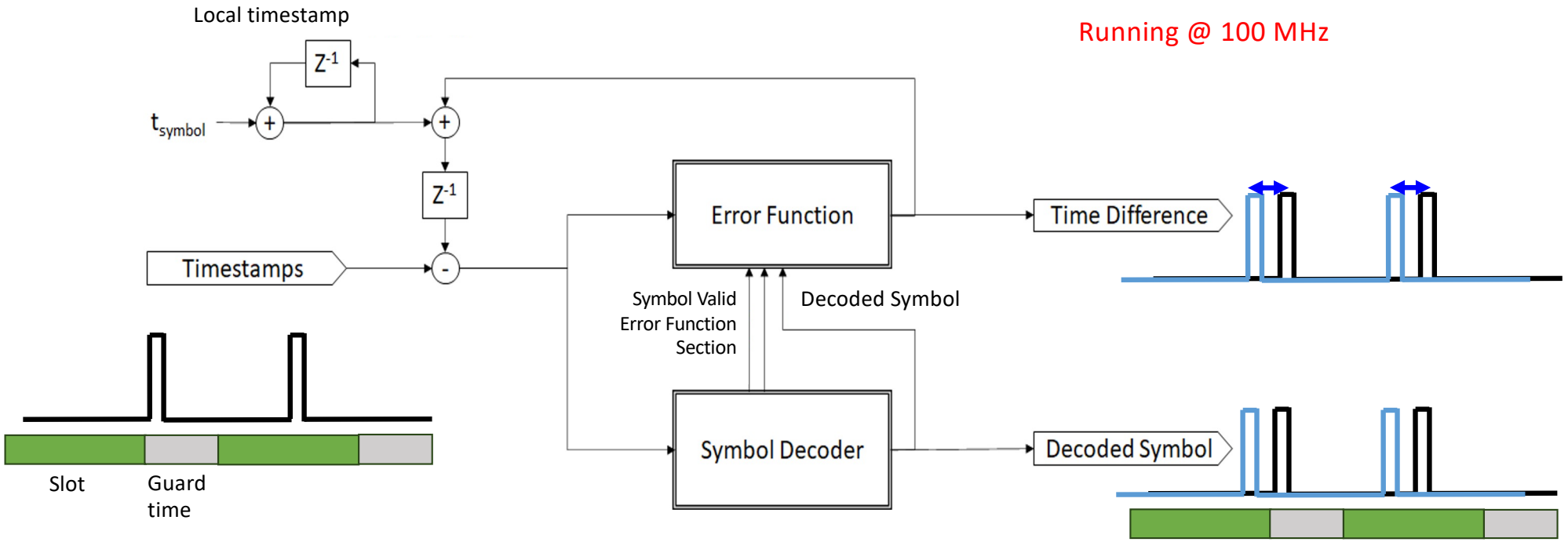
- 4 timestamps per pulse



- Two comparators with different thresholds and 4 latches

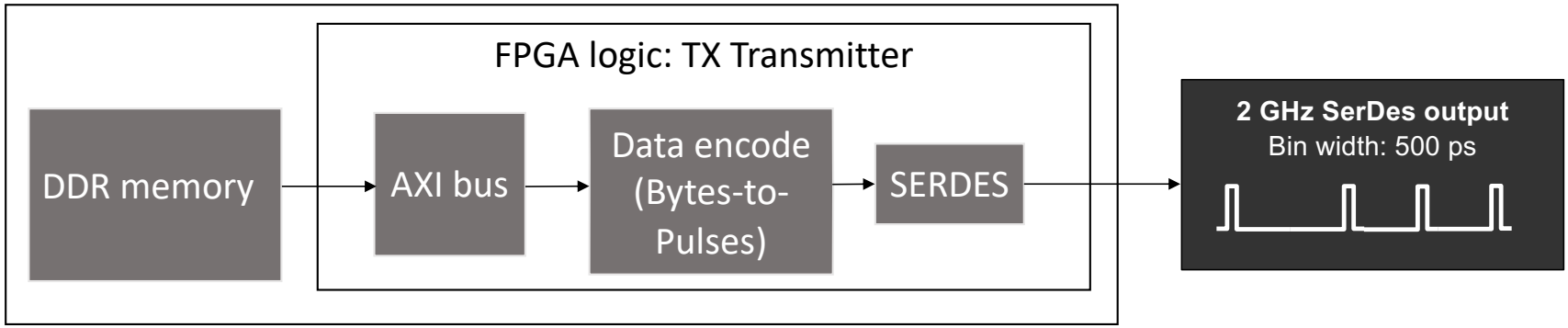


TDC Receiver: Decoder



TX Modulator

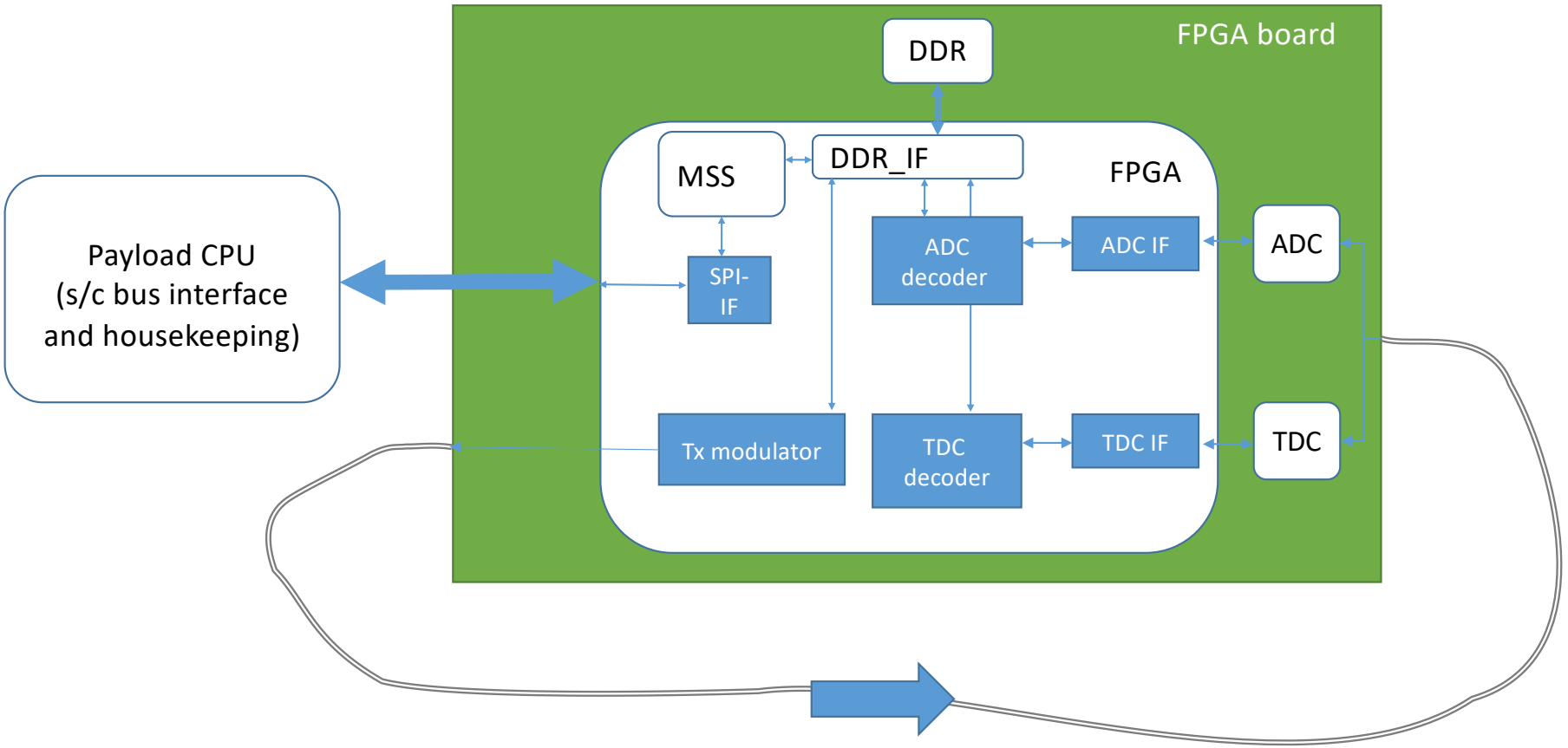
- Converts raw bytes into PPM symbols
- Output via SERDES



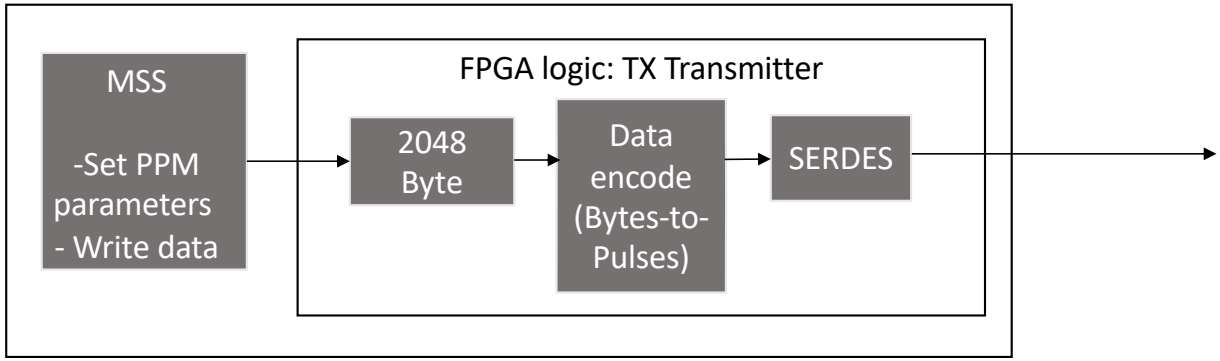
Raw bytes:
0001 1101 0011 1110 ….

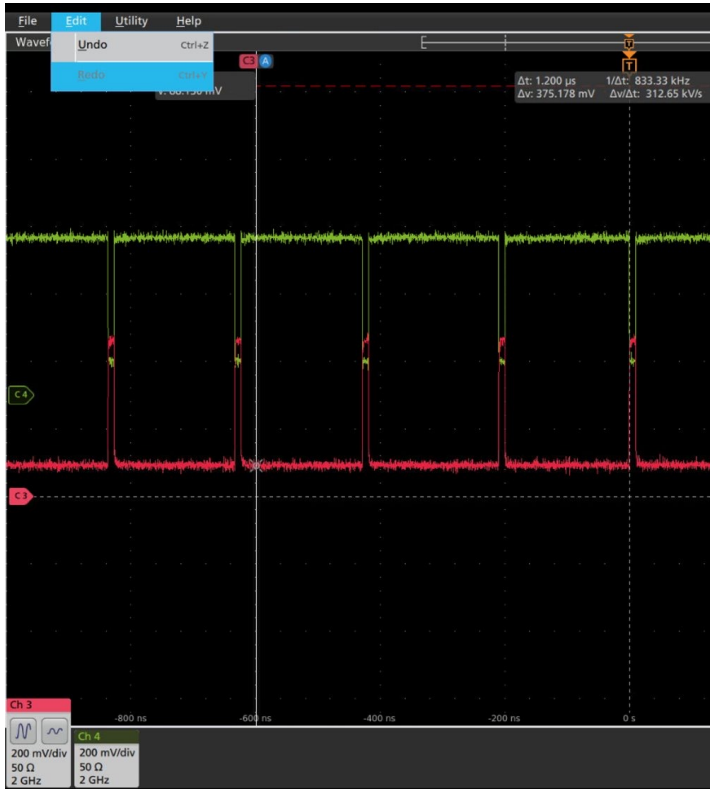
PPM16 symbols:
1 13 3 14 …

TDC Loopback Testing (LT)



TDC LT: Status TX Modulator





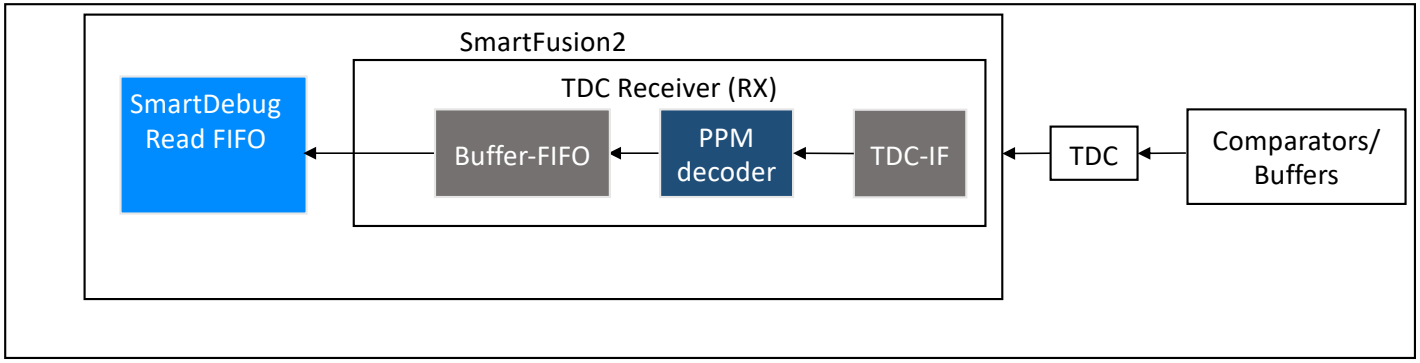
- Currently issues with DDR bus
  -> Instead: shorter test pattern in FIFO

TDC LT: Status Receiver

- Currently issues with DDR interface

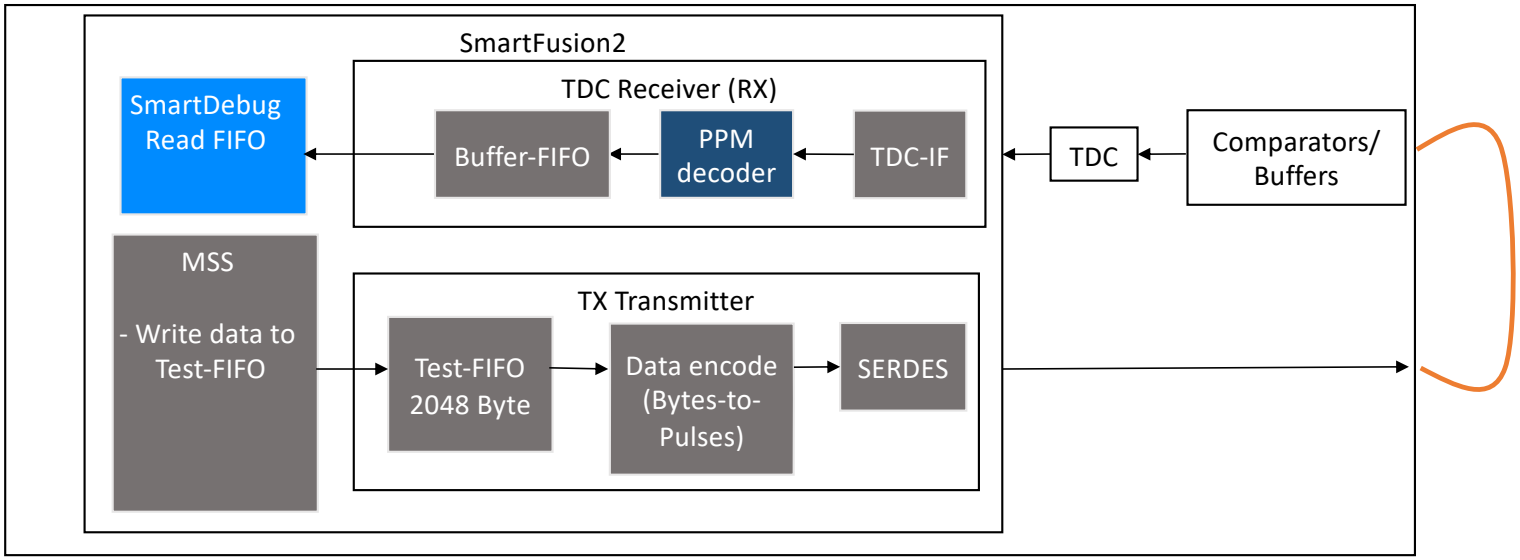
-> readout via JTAG/SmartDebug

- Currently only one TDC channel utilized



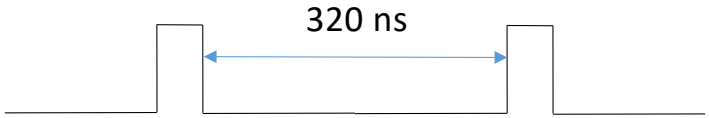
TDC LT: Overall status

- Testing:
  - Raw timestamp readout
  - Easy target data to check decoder (dark blue)



TDC LT Results: Raw Timestamps

- Test pulses timed to interval of 320 ns



- With LSB 4.88 ps:

-> expect increment of 21th bit for every 16th timestamp

3
0000BF38372F5683
0000BF38373F56AD
0000BF38374F569C
0000BF38375F55FE

User Design Memory Block: FABRIC_MODULES_0/RX_TDC_MODULE_0/TDCReceiver_0/TDC_AXI_TAP_0/TDC_TAP_BurstBuffer_0/T ... rapper_1/U2_asyncnonpipe
Port Width: 64-bit
Port Used: Port A

	0	1	2	3	4	5	6	7	8
0000	0000BF38378354C4	0000BF38376D54DD	0000BF38372E55C6	0000BF38372F5683	0000BF38373055C0	0000BF3837315566	0000BF3837325C3D	0000BF38373354CA	0000BF383
0010	0000BF38373C566B	0000BF38373D5696	0000BF38373E56B6	0000BF38373F56AD	0000BF383740568B	0000BF3837415652	0000BF38374255F2	0000BF38374355A1	0000BF383
0020	0000BF38374C55AF	0000BF38374D560E	0000BF38374E565A	0000BF38374F569C	0000BF38375056DC	0000BF38375156D5	0000BF38375256B5	0000BF383753567E	0000BF383
0030	0000BF38375C550C	0000BF38375D554B	0000BF38375E55A0	0000BF38375F55FE	0000BF383760566B	0000BF38376156B9	0000BF38376256E4	0000BF38376356F0	0000BF383

TDC LT Results: Decoder

Send data, easy target: 0000000E0000000E

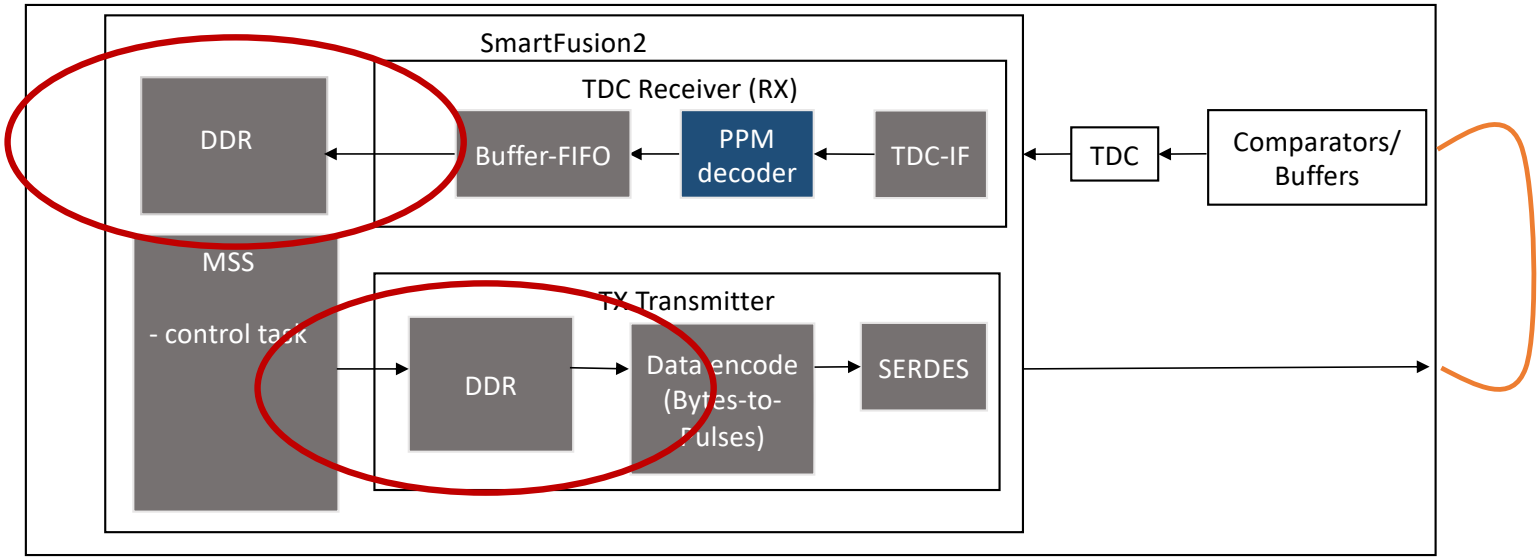
User Design Memory Block: FABRIC_MODULES_0/RX_TDC_MODULE_0/TDCReceiver_0/TDC_AXI_TAP_0/TDC_Decode_BurstBuffer_0/TDC_TAP_BurstBuffer_0/RW2.UI_ram_wrapper_1/U2_asyncnonpipe
Port Width: 64-bit
Port Used: Port A

	0	1	2	3	4	5	6	7	8
0000	00830D8300000D83	00000D0000000D00	00000D0000000D00	00000D0000000F00	00000D0000000C00	00000C0000000D00	00000D0000000D00	00000D0000000D00	00000D0000(
0010	00000D0000000E00	00000D0000000D00	00000D0000000D00	00000D0000000D00	00000D0000000D00	00000D0000000D00	00000D0000000D00	00000D0000000D00	00000D0000(
0020	00000D0000000D00	00000D0000000D00	00000D0000000D00	00000D0000000D00	00000D0000000D00	00000D0000000D00	00000D0000000D00	00000D0000000F00	00000D0000(
0030	00000D0000000D00	00000D0000000D00	00000D0000000D00	00000D0000000D00	00000D0000000D00	00000D0000000D00	00000D0000000D00	00000D0000000D00	00000D0000(

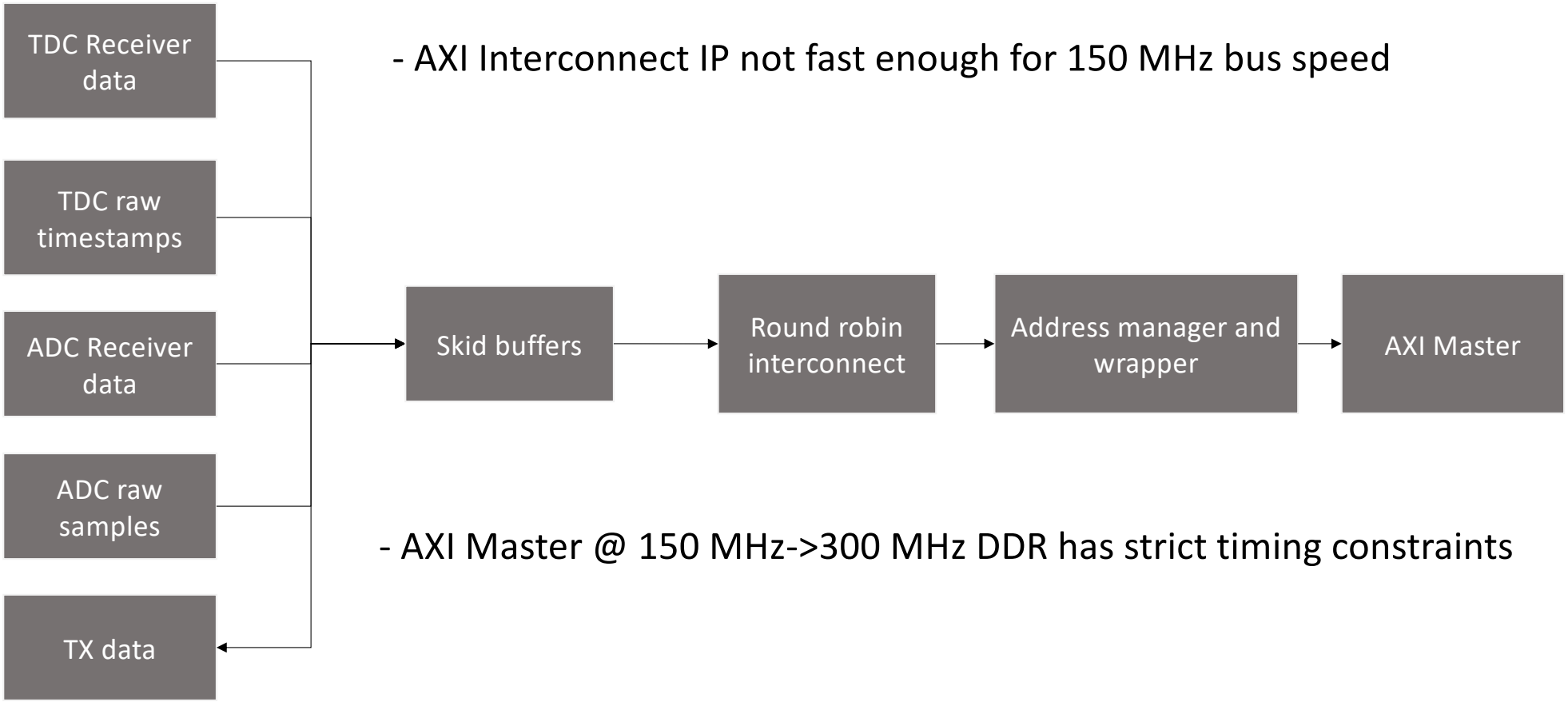
7
00000D0000000D00
00000D0000000D00
00000D0000000F00
00000D0000000D00

Data is detected but offset of 1 symbol and occasional bit error

Next steps


SmartFusion2
TDC Receiver (RX)
DDR
Buffer-FIFO
PPM decoder
TDC-IF
TDC
Comparators/ Buffers
MSS
- control task
TX Transmitter
DDR
Data encode (Bytes-to-Pulses)
SERDES

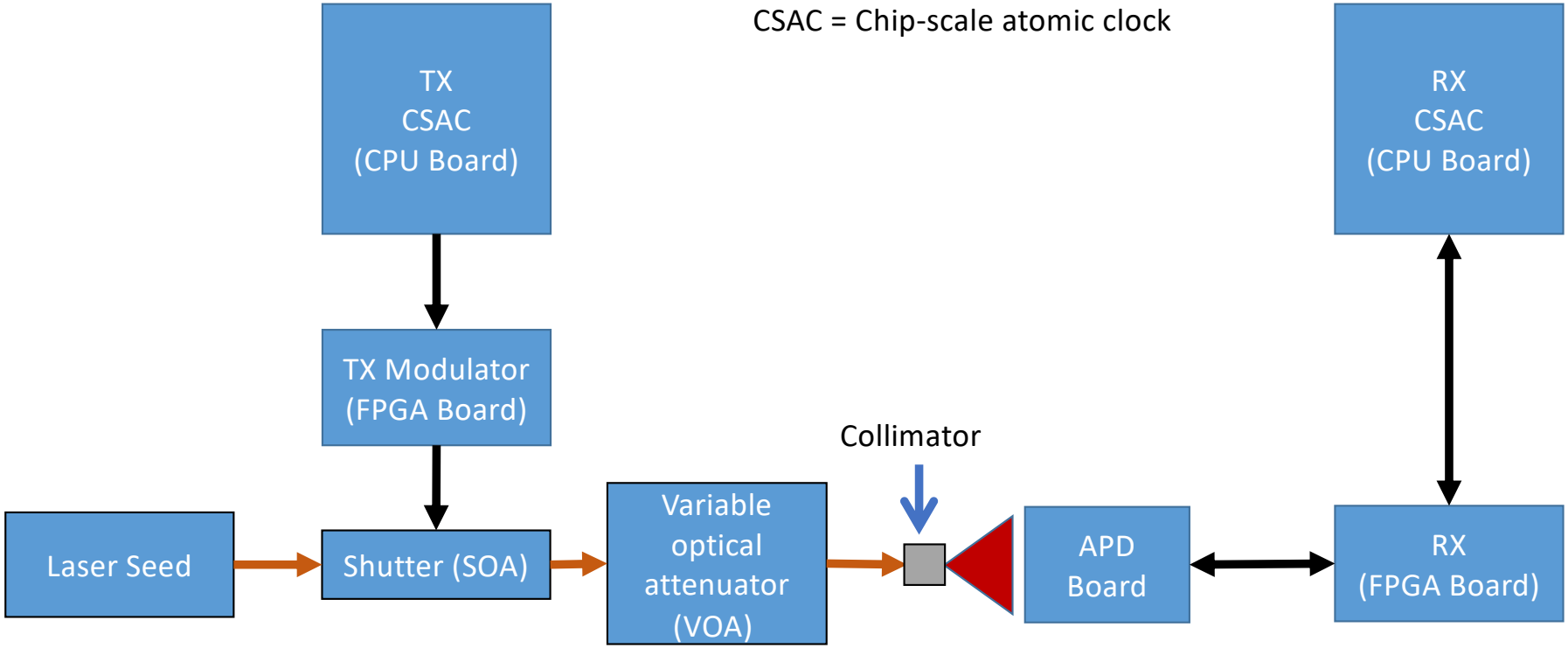
Next steps: custom interconnect



- AXI Interconnect IP not fast enough for 150 MHz bus speed

- AXI Master @ 150 MHz->300 MHz DDR has strict timing constraints

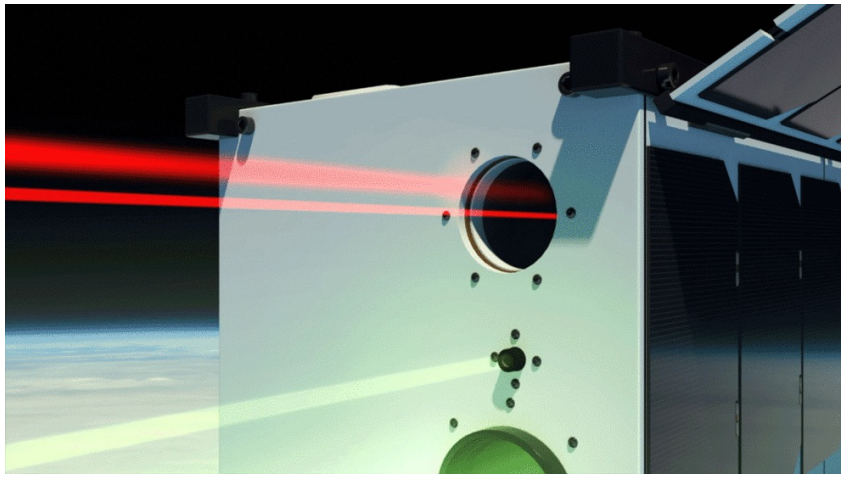
Next steps: optical flatsat



Summary

CLICK B/C Mission

- CubeSats with low SWaP + COTS components
- full-duplex, high data rate laser com, ranging, timing transfer



TDC-based data & timing transfer

- TDC timestamps PPM pulses 4 times
- Tracking loop for PPM decoder (100 MHz)
- Flatsat: First successful electric loopback tests
- Future: optical flatsat, independent clocks

CLICK B/C Launch: Early 2025

Thank you!

This research is supported by NASA grant 80NSSC18K1579. Thanks to the NASA Ames management team and Massachusetts Institute of Technology Space Telecommunications, Astronomy, Radio (STAR) Laboratory for their support of this research.

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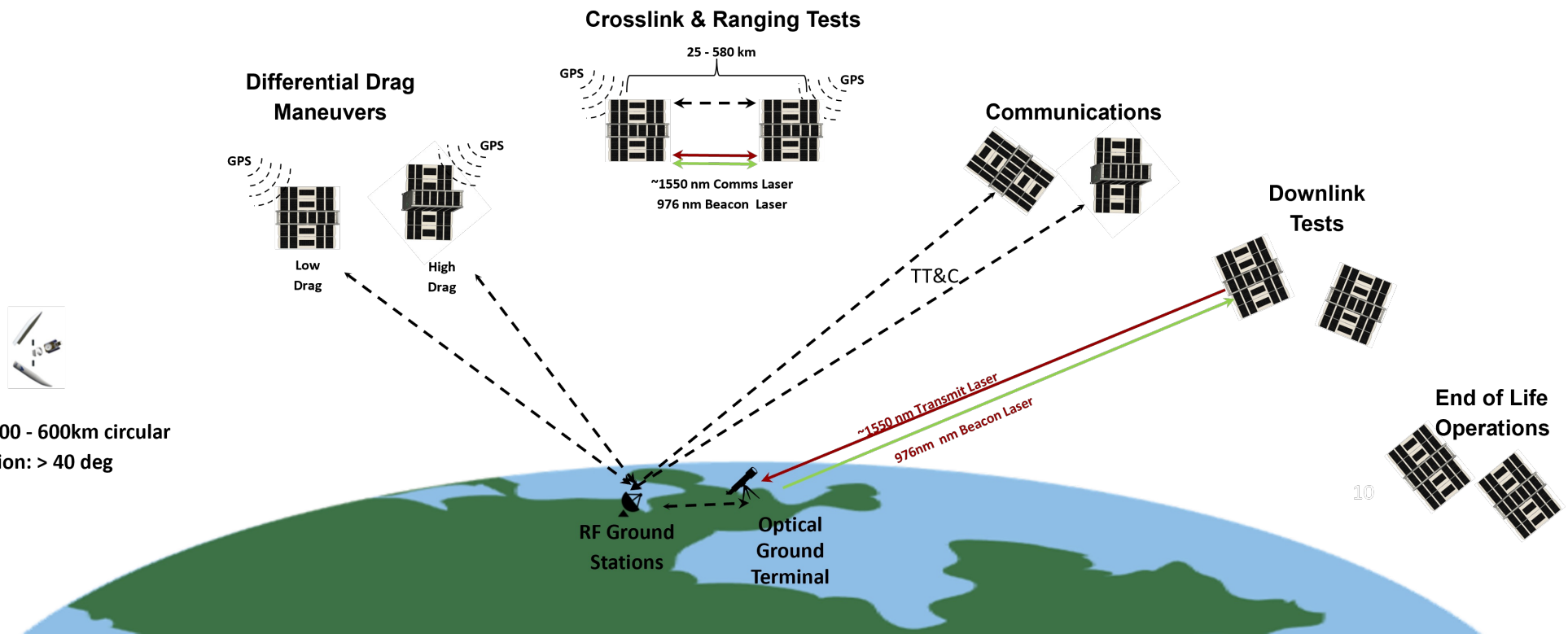
Backup slides

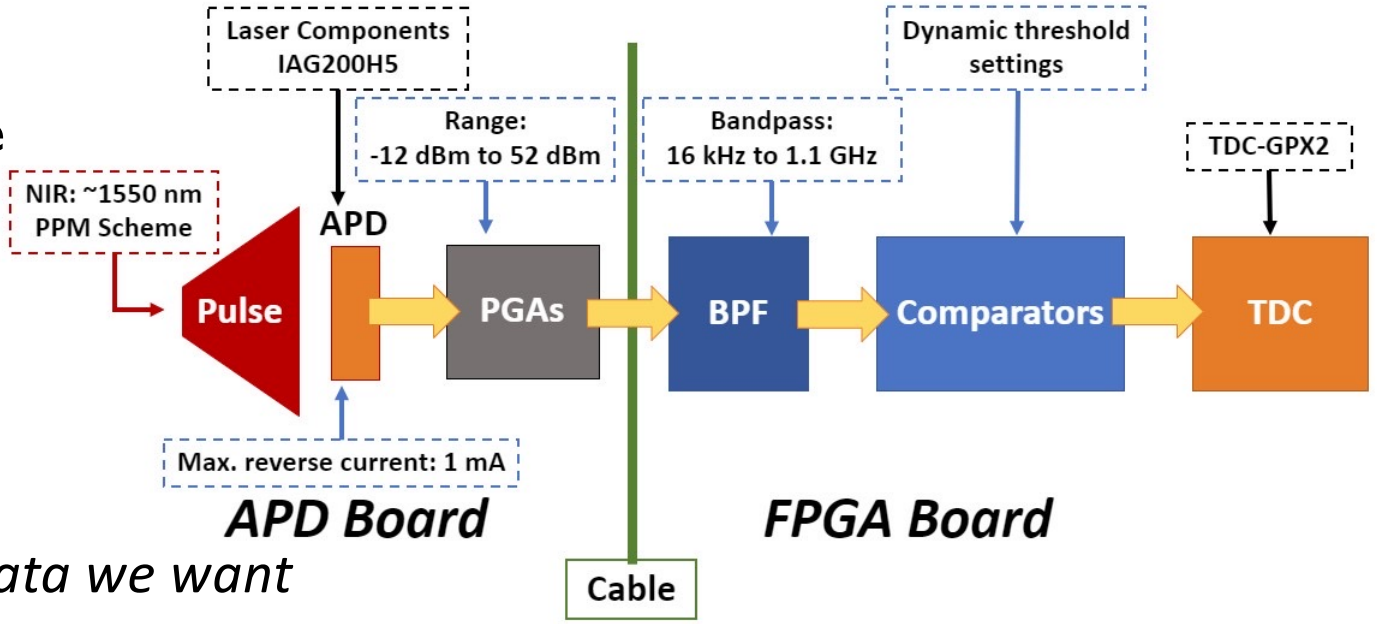
CLICK B/C CONOPS



Orbit: 400 - 600km circular
Inclination: > 40 deg

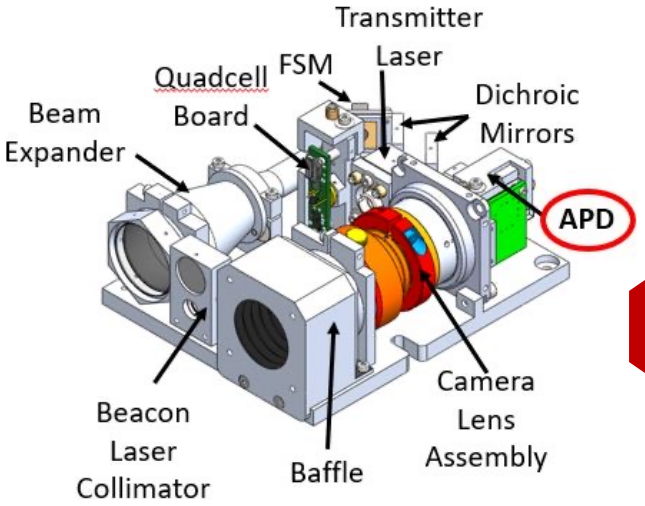
APD-TDC Receiver Chain

- TDC samples: 2 on the rising edge at set thresholds, and 2 at the falling edge (same thresholds)
- FPGA converts TDC measurements into a timestamp
- PPM decoding requires knowing pulse timing

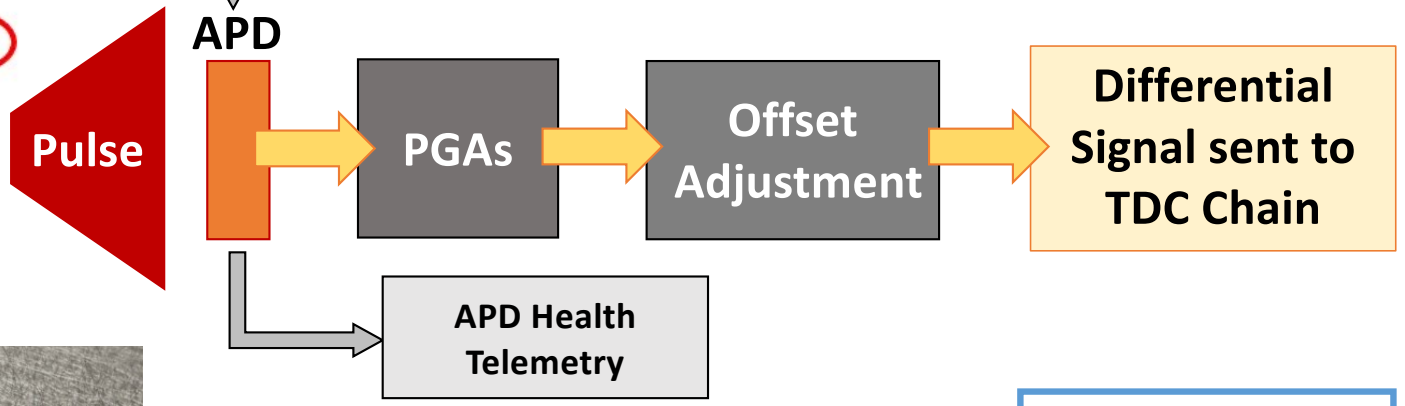


The data we want

APD Board



Coogan, 2022. Small Satellite Conference.



High Voltage Bias:
- Min. operational: ~60 V
- Breakdown: ~71 V

Telemetry:
- 3 temperature readings
- APD Vrssi (Received Signal Strength Indicator voltage)

- **System Health Monitoring**
- **Mission Ops Development**

✓ **NEP Requirement: 15 pW/$\sqrt{\text{Hz}}$**

Flatsat/Testbed Development

✓Initial pulse testing capabilities confirmed

Next Steps:

- Upgrade laser TX system
- Optical loopback testing
- End-to-end testbed performance testing (CSAC in loop)