Kyutech
Kyushu Institute of Technology
国立大学法人
九州工業大学

La SEINE
Laboratory of
Lean
Satellites
Enterprises and
IN-orbit
Experiments

Programmable Interface Board for Higher CubeSat Form Factor and Complex Mission Payload

2021 CUBESAT DEVELOPERS WORKSHOP

Marloun Sejera*, Takashi Yamauchi, Yukihisa Otani, Mengu Cho

La SEINE, Kyushu Institute of Technology (Kyutech), Japan

Kyutech BIRDS Project

- Acronym for Joint Global Multi-Nation BIRDS Satellite Project
- Targets non-space fairing countries
- Build, test, launch and operate 1U CubeSats in two years

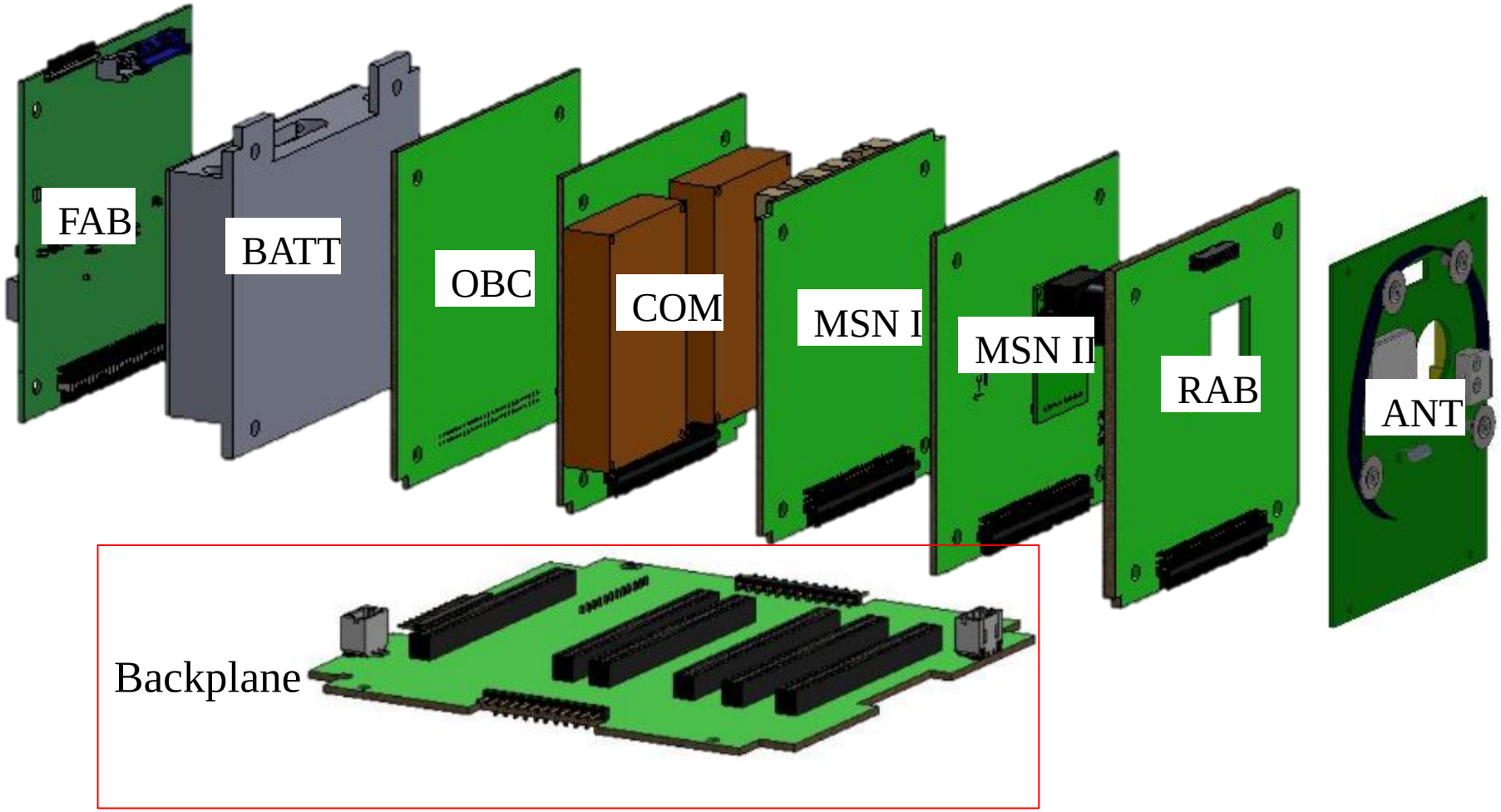
BIRDS-1	BIRDS-2	BIRDS-3	BIRDS-4	BIRDS-5
Japan	Japan	Japan	Japan	Japan
Ghana*	Bhutan*	Nepal*	Paraguay*	Uganda*
Mongolia*	Malaysia	Sri Lanka*	Philippines	Zimbabwe*
Nigeria	Philippines			
Bangladesh*				

*country's first satellite

BIRDS Standard Bus System

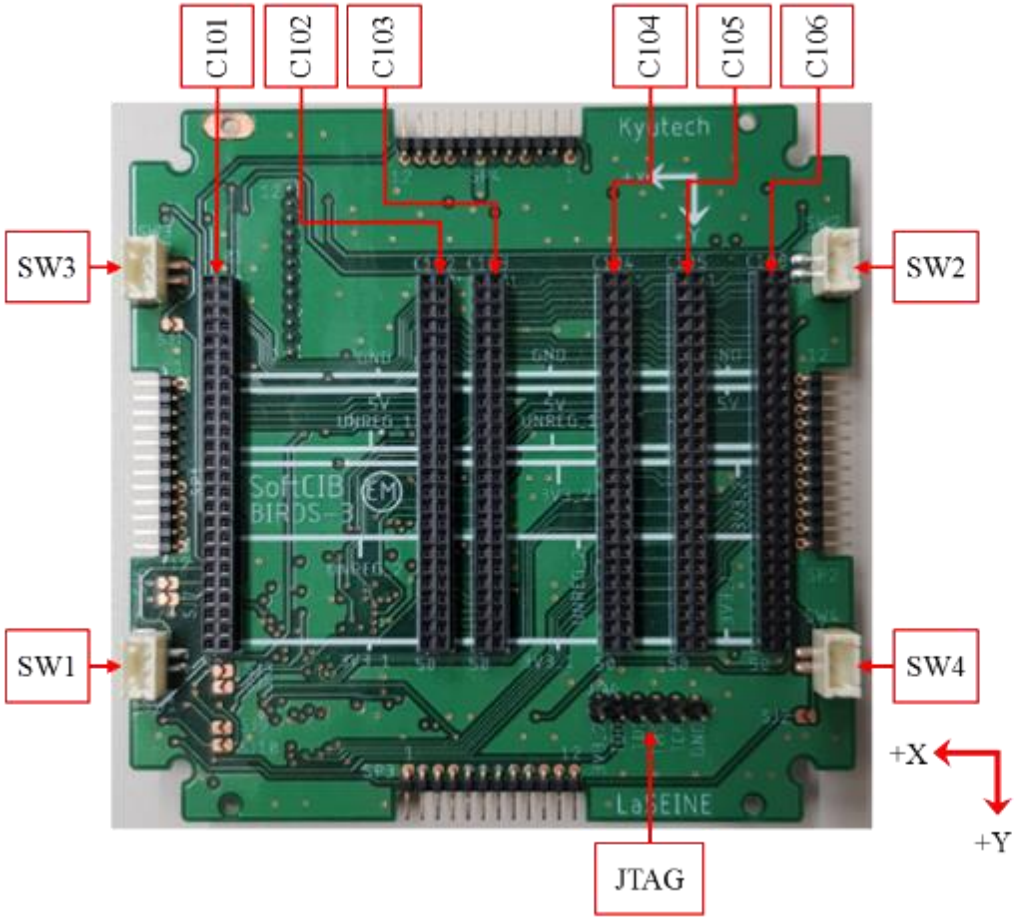
Implemented backplane approach

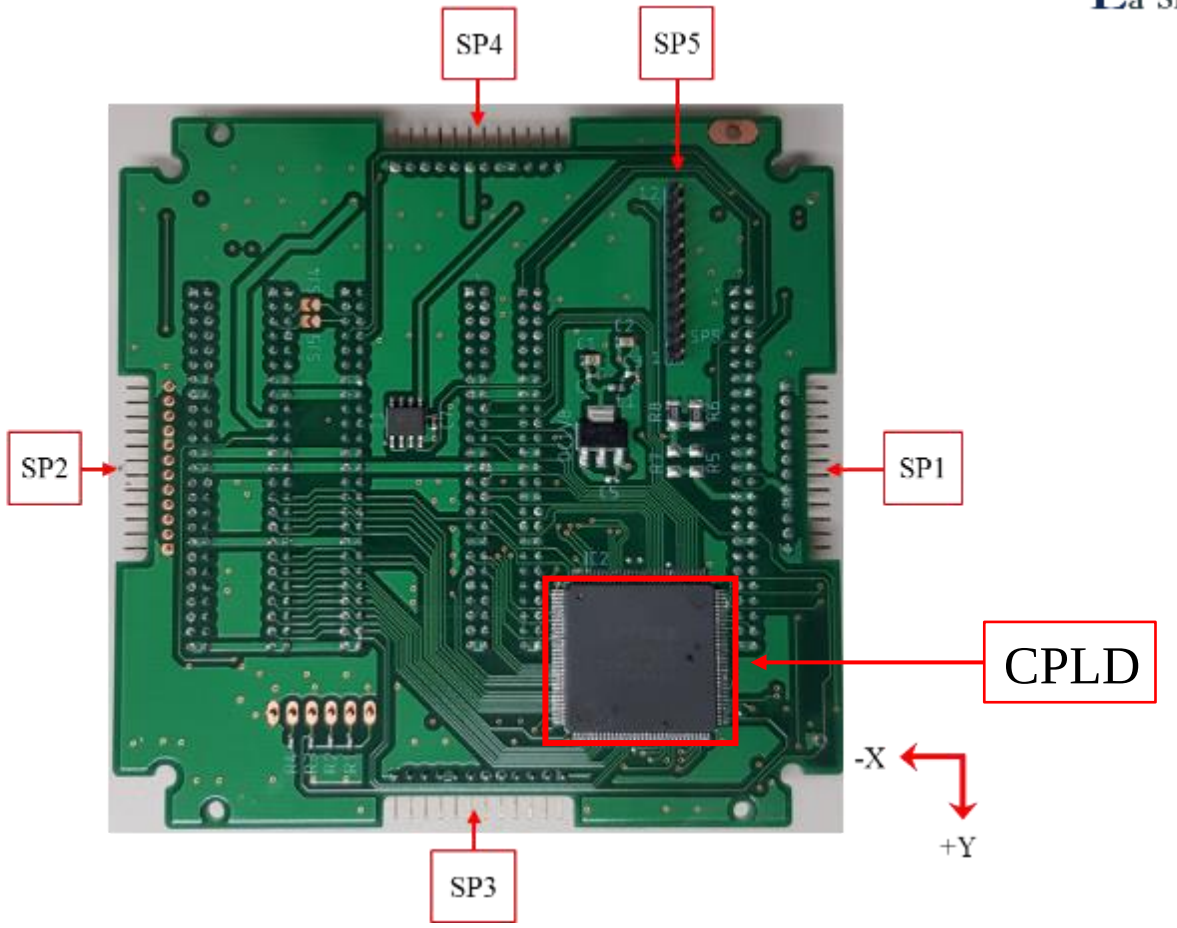
- reduce use of harness
- smaller connectors
- easy to integrate and disassemble



BIRDS CubeSat internal view

BIRDS Configurable Backplane

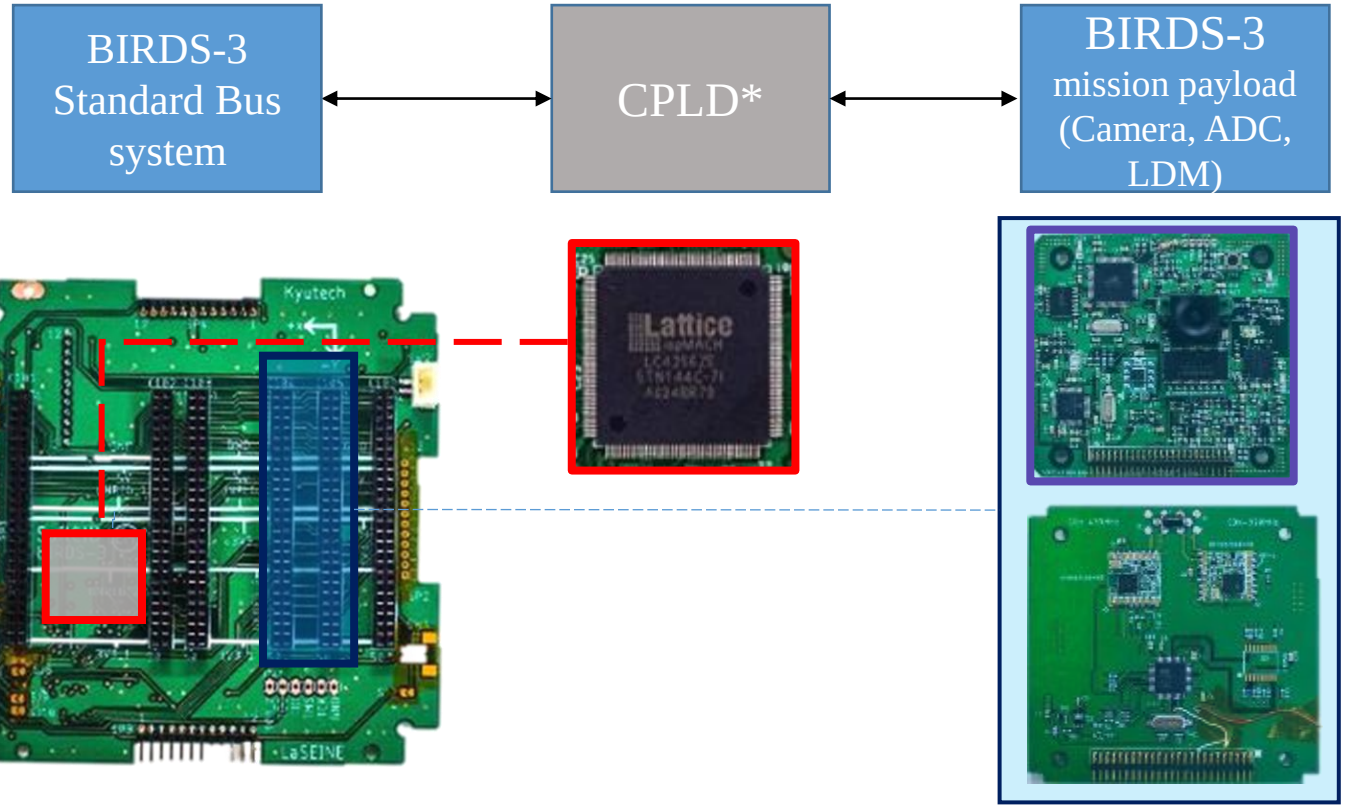




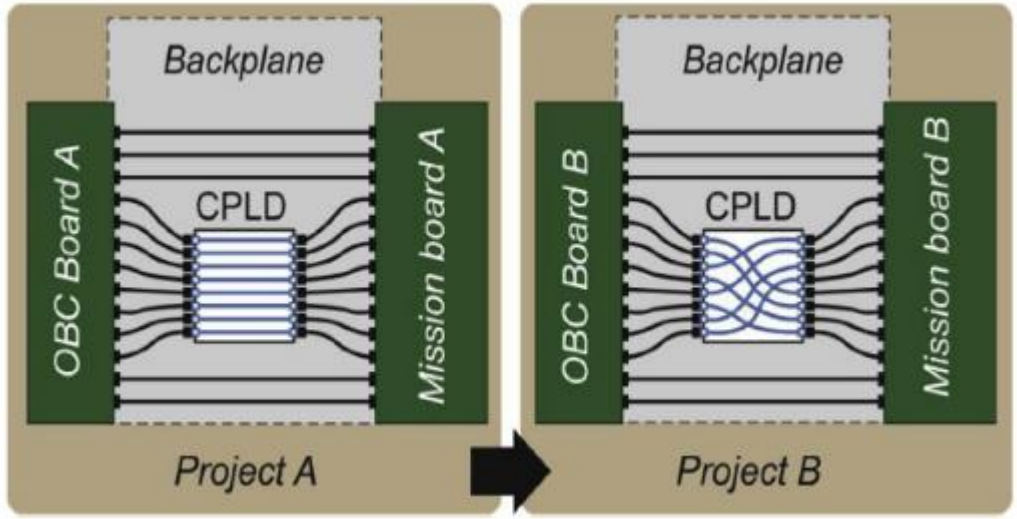
- 6x 50-pin board connectors (C101-C106)
- 4x 2-pin deployment switch connectors (SW1-SW4)
- 5x 12-pin panel connectors (SP1-SP5)
- 1x JTAG for CPLD programming

BIRDS Configurable Backplane

❑ Routing between system bus and mission payload is done by re-programming CPLD.



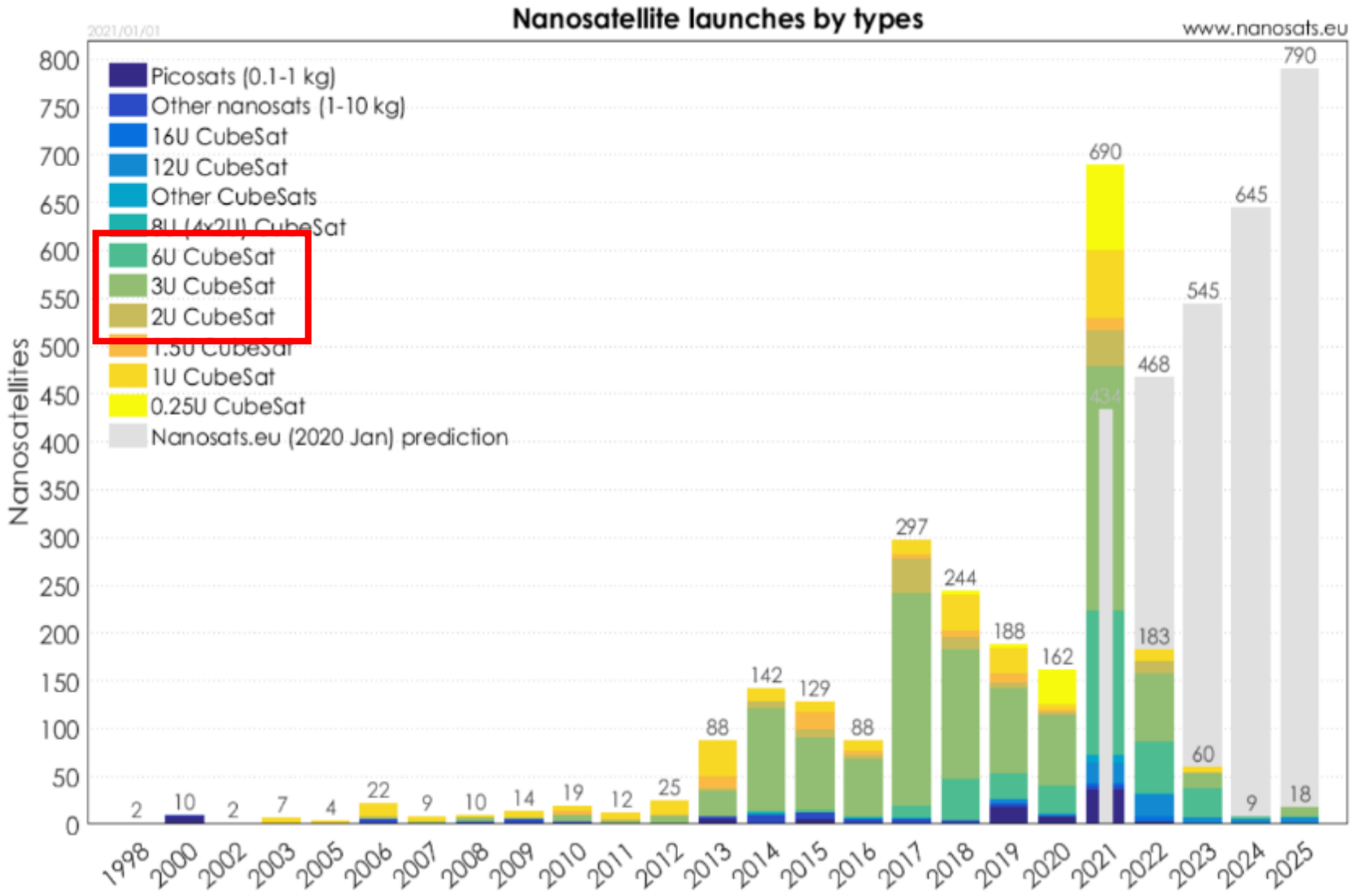
*Complex Programmable Logic Device



Tumenjargal, T., Kim, S., Masui, H., Cho, M., CubeSat bus interface with Complex Programmable Logic Device, Acta Astronautica Vol. 160, 2019, pp. 331-342

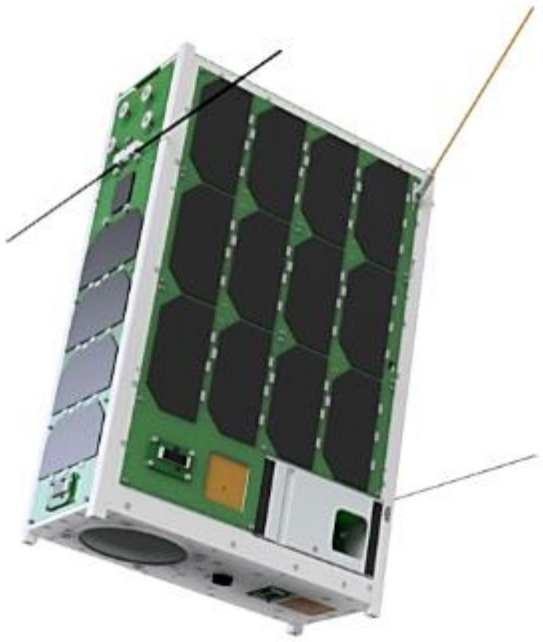
Moving up

- More launch opportunities on bigger CubeSats
- Need to demonstrate the scalability of programmable interface board

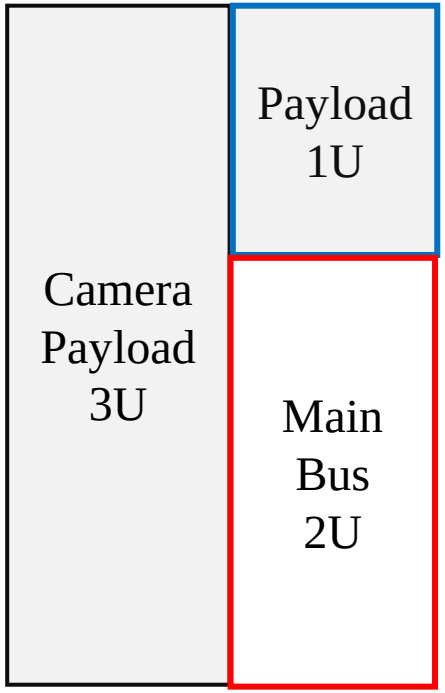


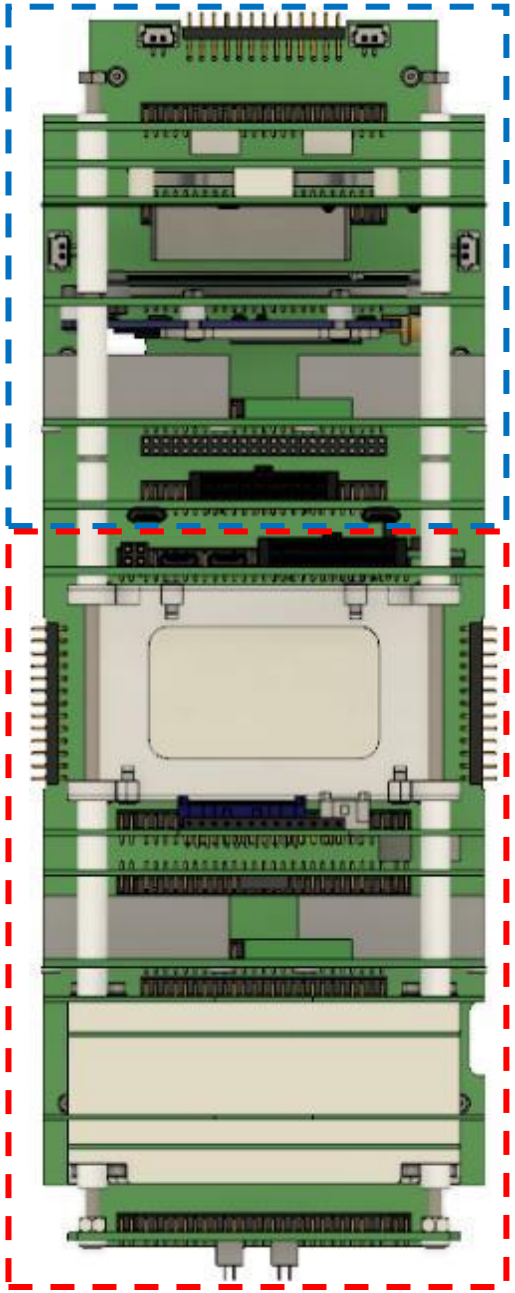
Source: https://www.nanosats.eu/img/fig/Nanosats_years_types_2021-01-01.png

6U CubeSat

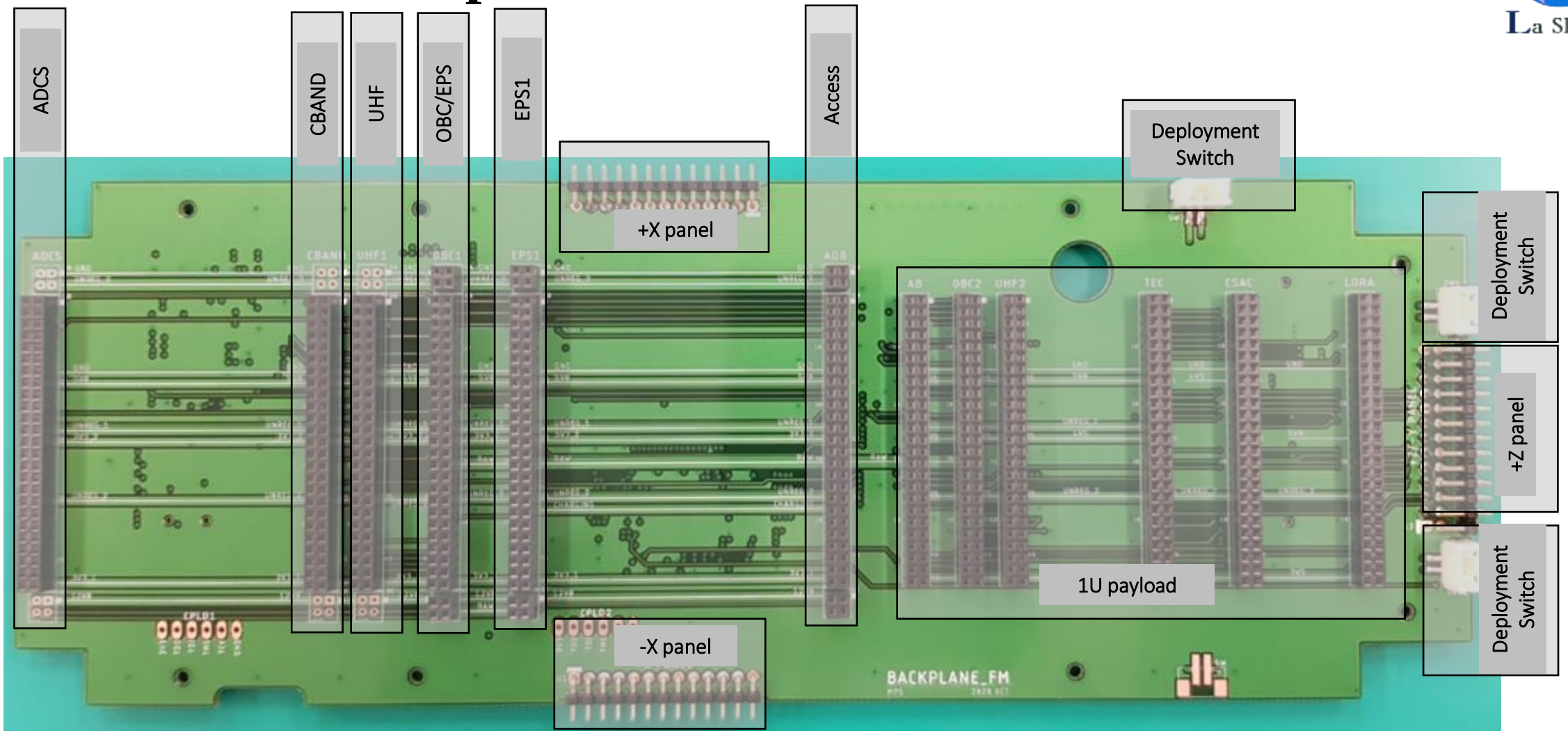


- 3 sections: 3U Camera payload, 1U payload, and 2U main bus
- Sections are inter-connected through backplane



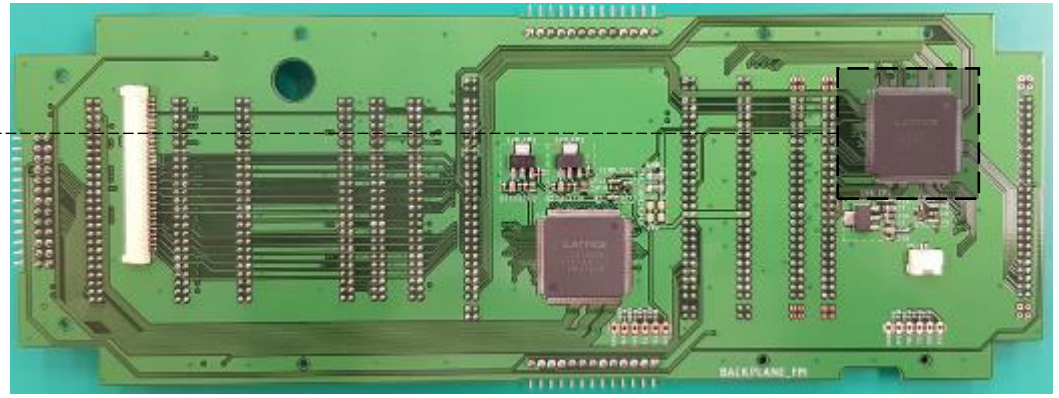


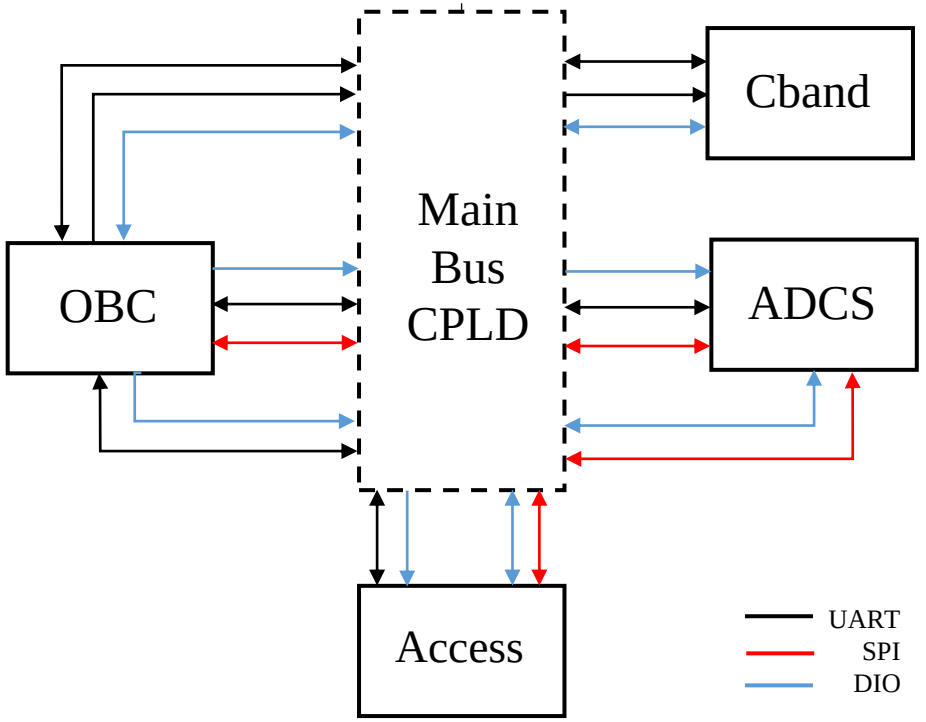
6U CubeSat Backplane



- 12x 50-pin board connectors (6x main bus + 6x payload)
- 6x 4-pin board connectors
- 3x 2-pin deployment switch connectors
- 3x panel connectors (2x 12-pin, 1x 25-pin)
- 2x JTAG for CPLD programming

6U CubeSat Backplane

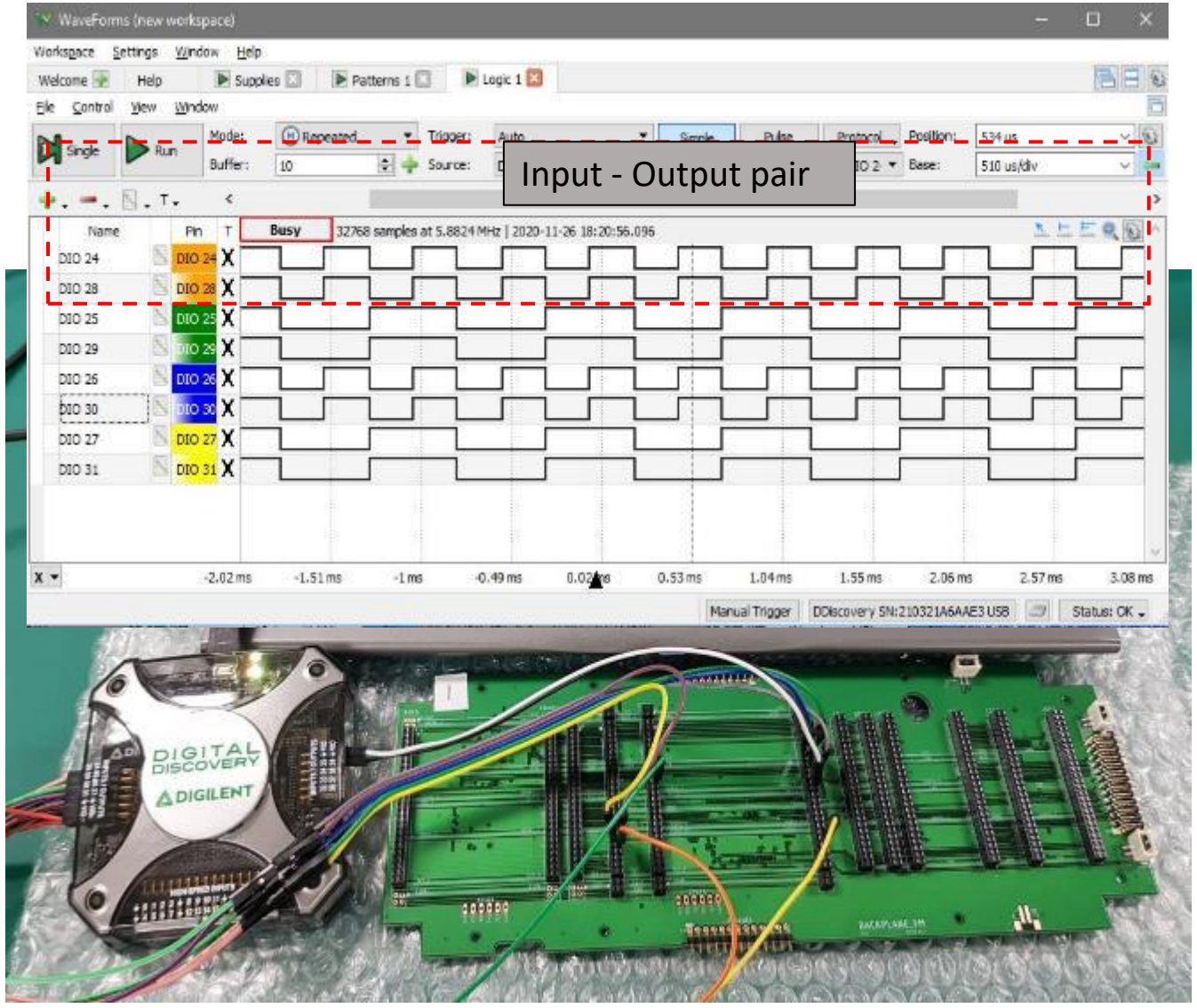




FROM			TO		
Board	Pin	Description	Board	Pin	Description
OBC	37	OBC-ADB UART_1 (MainPIC_to_RelayPIC)	ADB	11	OBC-ADB UART_1 (MainPIC_to_RelayPIC)
ADB	12	OBC-ADB UART_1 (RelayPIC_to_MainPIC)	OBC	38	OBC-ADB UART_1 (RelayPIC_to_MainPIC)
ADB	21	ADB-EPS1 DIO (RelayPIC_to_MainBC)	EPS	21	ADB-EPS1 DIO (RelayPIC_to_MainBC)
EPS	22	EPS1-ADB BAT_VOLTAGE	ADB	22	EPS1-ADB BAT_VOLTAGE
OBC	42	OBC-ADB DIO (ONOFF MainPIC_to_RelayPIC)	ADB	41	OBC-ADB DIO (ONOFF MainPIC_to_RelayPIC)
ADCS	38	ADCS-ADB SS_MAG (ADCS_to_ADB)	ADB	43	ADCS-ADB SS_MAG (ADCS_to_ADB)
ADCS	39	ADCS-ADB MOSI_MAG (ADCS_to_ADB)	ADB	44	ADCS-ADB MOSI_MAG (ADCS_to_ADB)
ADB	45	ADCS-ADB MISO_MAG (ADB_to_ADCS)	ADCS	40	ADCS-ADB MISO_MAG (ADB_to_ADCS)
ADCS	41	ADCS-ADB SCLK_MAG (ADCS_to_ADB)	ADB	46	ADCS-ADB SCLK_MAG (ADCS_to_ADB)
ADCS	42	ADCS-ADB DRDY_MAG (ADCS_to_ADB)	ADB	47	ADCS-ADB DRDY_MAG (ADCS_to_ADB)
ADCS	43	ADCS-ADB Reset_MAG (ADCS_to_ADB)	ADB	48	ADCS-ADB Reset_MAG (ADCS_to_ADB)
OBC	10	OBC-ADCS DIO (ONOFF MainPIC_to_ADCS)	ADCS	10	OBC-ADCS DIO (ONOFF MainPIC_to_ADCS)
OBC	27	OBC-ADCS UART (MainPic_to_ADCS)	ADCS	27	OBC-ADCS UART (MainPic_to_ADCS)
ADCS	28	OBC-ADCS UART (ADCS_to_MainPic)	OBC	28	OBC-ADCS UART (ADCS_to_MainPic)
ADCS	31	OBC-ADCS SPI_CS (ADCS_to_FM2)	OBC	31	OBC-ADCS SPI_CS (ADCS_to_FM2)
ADCS	32	OBC-ADCS SPI _MOSI (ADCS_to_FM2)	OBC	32	OBC-ADCS SPI _MOSI (ADCS_to_FM2)
OBC	33	OBC-ADCS SPI_MISO (FM2_ to_ADCS)	ADCS	33	OBC-ADCS SPI_MISO (FM2_ to_ADCS)
ADCS	34	OBC-ADCS SPI_SCK (ADCS_to_FM2)	OBC	34	OBC-ADCS SPI_SCK (ADCS_to_FM2)
OBC	11	OBC-CBAND UART_1 (MainPIC_to_CBAND)	CBAND	41	OBC-CBAND UART_1 (MainPIC_to_CBAND)
CBAND	42	OBC-CBAND UART_1 (CBAND_to_MainPIC)	OBC	12	OBC-CBAND UART_1 (CBAND_to_MainPIC)
CBAND	40	OBC-CBAND RTS (CBAND_to_ComPIC)	OBC	40	OBC-CBAND RTS (CBAND_to_ComPIC)
OBC	41	OBC-CBAND UART_2 (ComPIC_to_CBAND)	CBAND	39	OBC-CBAND UART_2 (ComPIC_to_CBAND)
OBC	43	OBC-CBAND CW (ComPIC_to_CBAND)	CBAND	46	OBC-CBAND CW (ComPIC_to_CBAND)

- 22 pairs of connections (UART, SPI and DIO) routed through main bus CPLD
- 1u payload has its dedicated CPLD for routing digital signals

CPLD code and verification



ispLEVER Project Navigator - [KITSUNE_EM_MAINBUS_CPLD.syn]

File View Source Process Options Tools Window Help

Sources in Project:

- KITSUNE_EM_MAINBUS_CPLD
- Documents
- LC4256ZE-7TN144I
- [MAINBUS_CPLD (kitsune_em_mainbu

Processes for current source:

- Hierarchy Browser
- Lattice Synthesize VHDL File
- Compile EDIF File
- Compiled Equations

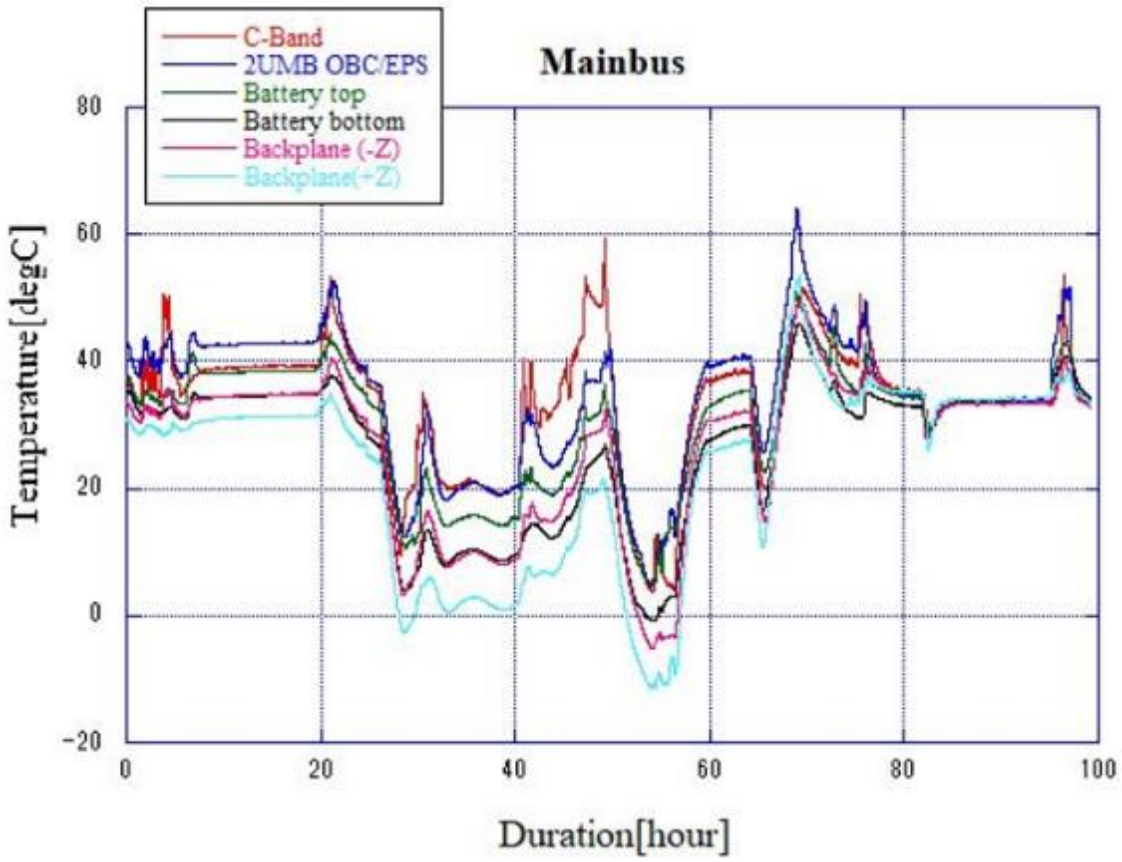
Text Editor - [kitsune_em_mainbus_cpld.vhd]

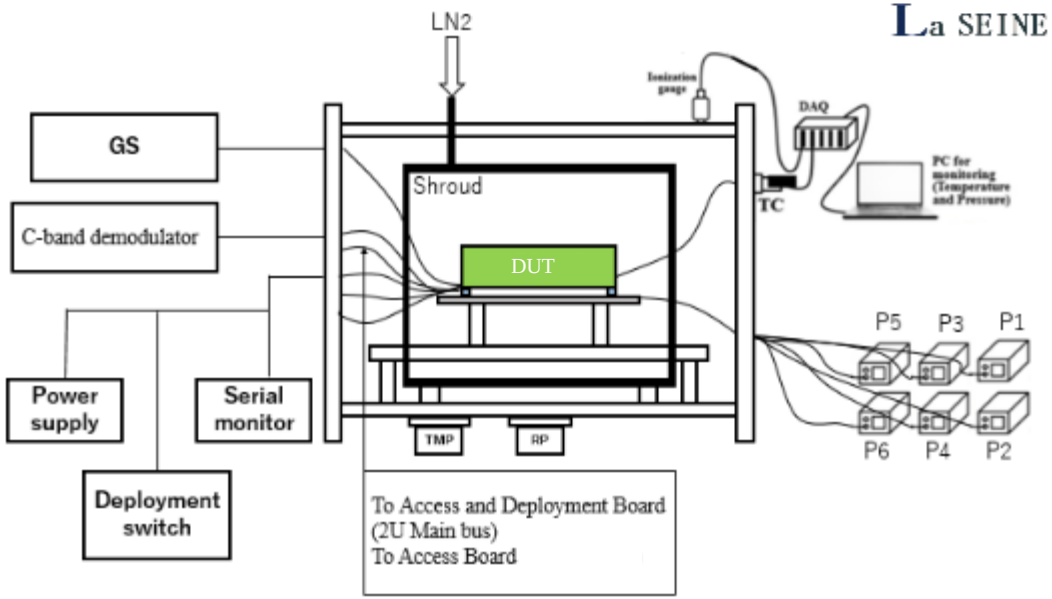
File Edit View Templates Tools Options Window Help

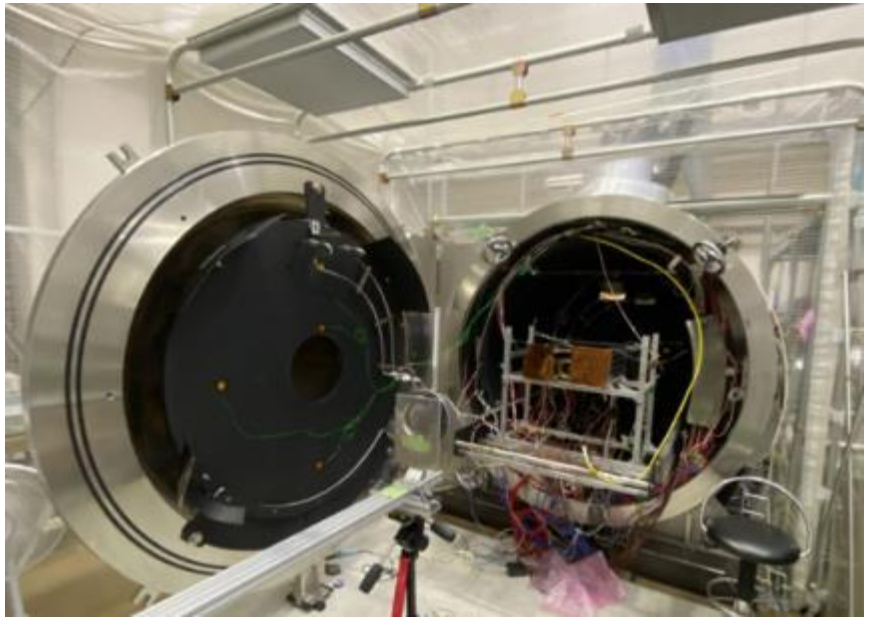
```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;
library MACH;
use MACH.components.all;

entity MAINBUS_CPLD is
  port  (
        cpld_IN: in std_logic_vector (0 to 21);
        cpld_OUT: out std_logic_vector (0 to 21)
        );
  end;

architecture MAINBUS of MAINBUS_CPLD is
  begin
        cpld_OUT <= cpld_IN;

  end MAINBUS;
```

- ❑ Voltage/ Signal follower using VHDL code.
- ❑ Input-output signal pair was verified using logic analyzer.

Thermal vacuum test





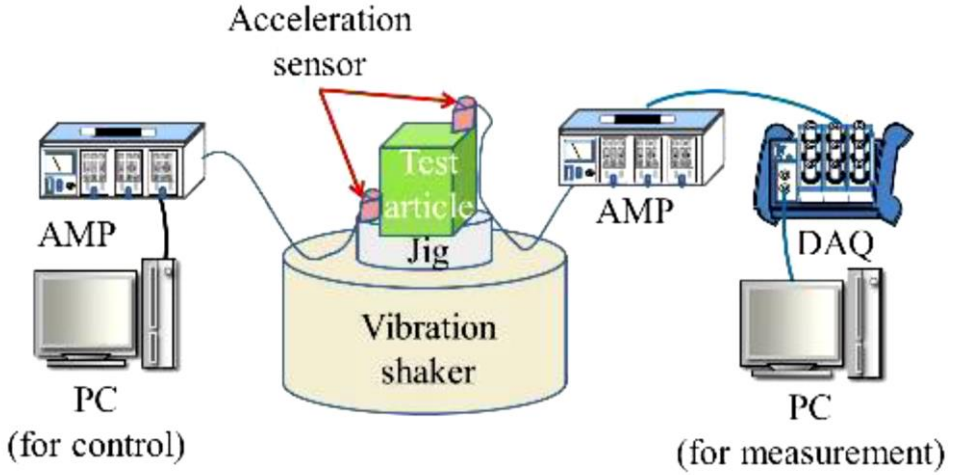


- Worst hot: +60°C
- Worst cold: -15°C
- Cycles: 2

Vibration Test

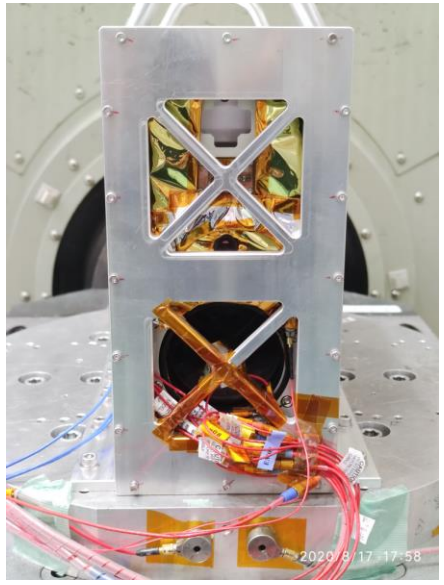
Random Vibration QT Profile

Envelope (QT)	
Freq. (Hz)	**PSD (g2/Hz)**
20	0.04
50	0.04
120	0.062
230	0.062
1000	0.009
2000	0.0026
Overall (Grms)	5.77
Duration (s)	120

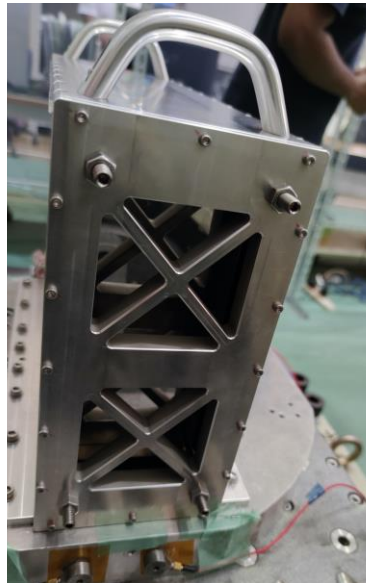


Sine Burst Vibration QT

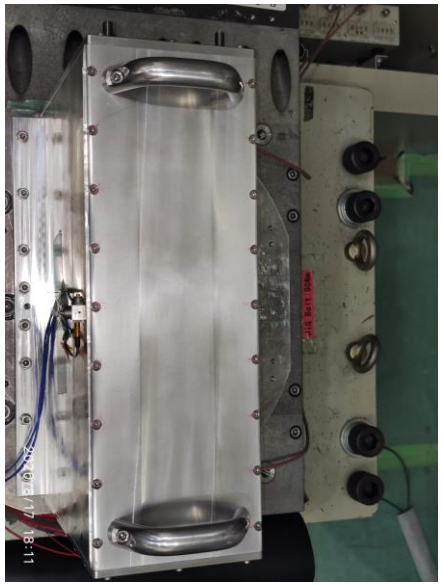
SINE BURST QT			
Direction	**Freq. [Hz]**	**QT**	
		Number of waves	**Acceleration [G]**
Vertical axis (Y)	10~40	10 or more	11.25
Horizontal axis (X, Z)	10~40		11.25
			11.25



(a) -Z axis-Front view



(b) +Z axis Back view

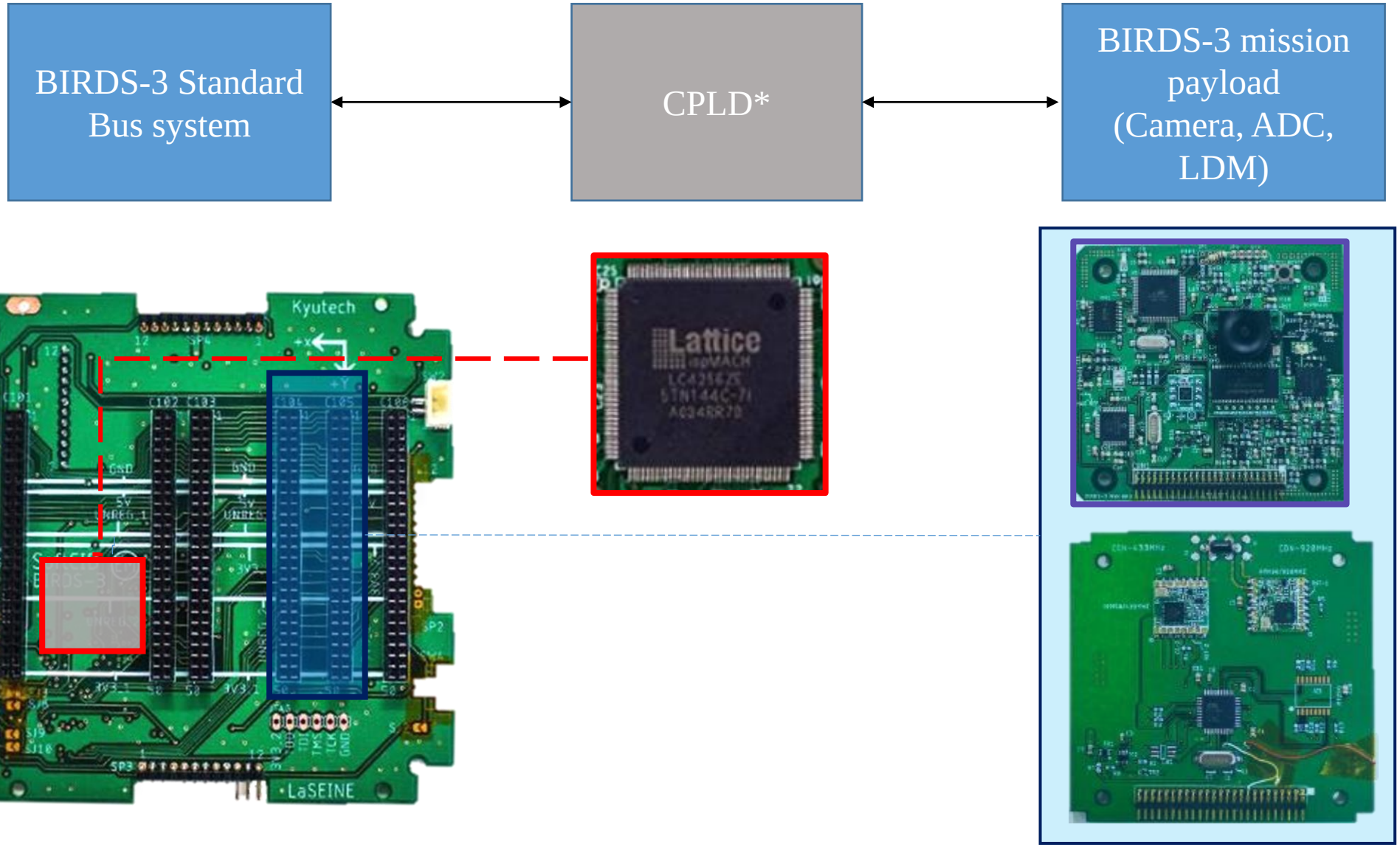


(c) +Y axis- Top view

Summary

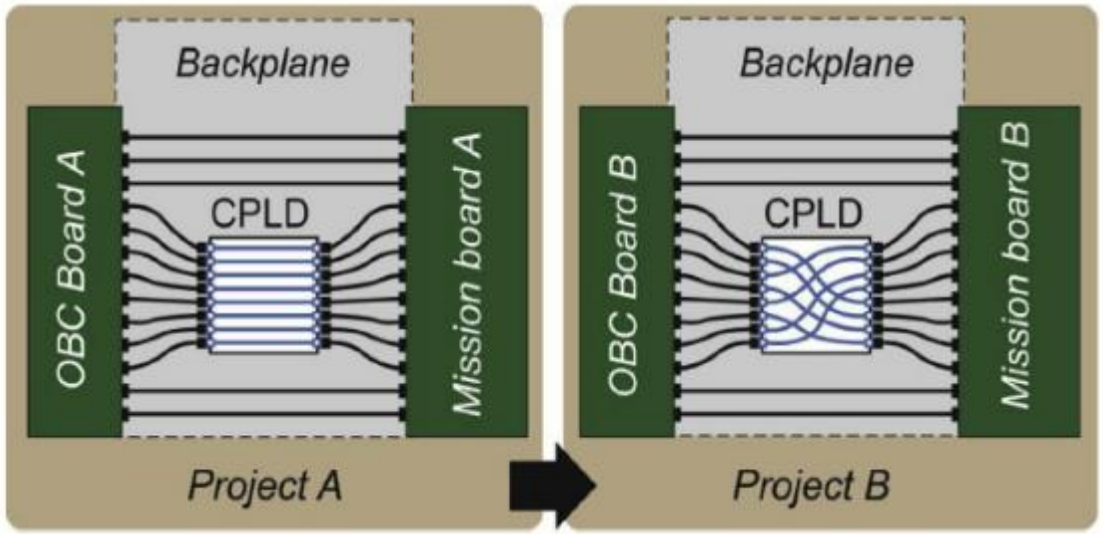
- A backplane was designed to demonstrate the scalability of programmable interface board.
- It is used in a 6U CubeSat which houses a 3U camera payload, 2U main bus and a 1U payload.
- Complex programmable logic device (CPLD) ICs were used to route digital lines within the backplane. CPLD has flight heritage from BIRDS project.
- The satellite passed space environment tests (i.e. TVT and vibration test)
- The satellite is targeted to launch by end of the year.

Platform-payload interface



*Complex Programmable Logic Device

Gap



Tumenjargal, T., Kim, S., Masui, H., Cho, M., CubeSat bus interface with Complex Programmable Logic Device, Acta Astronautica Vol. 160, 2019, pp. 331-342

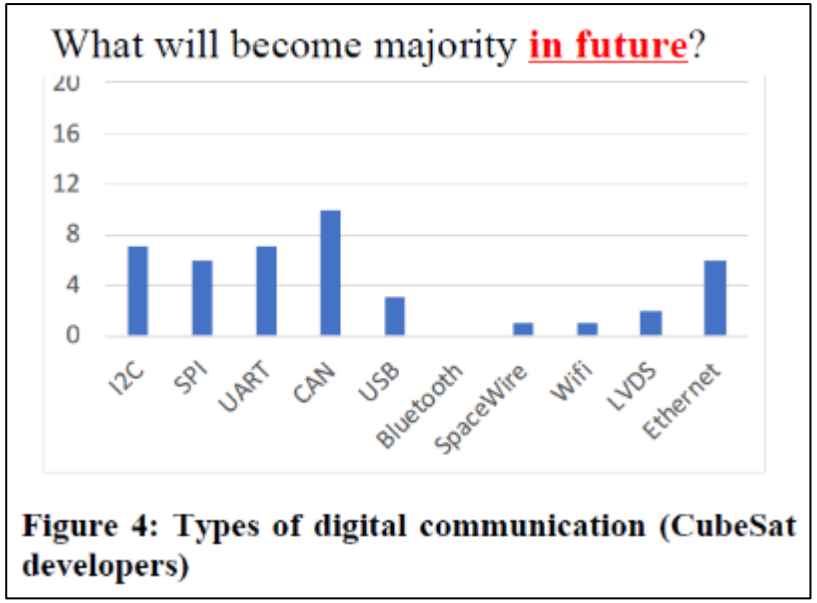


Figure 4: Types of digital communication (CubeSat developers)

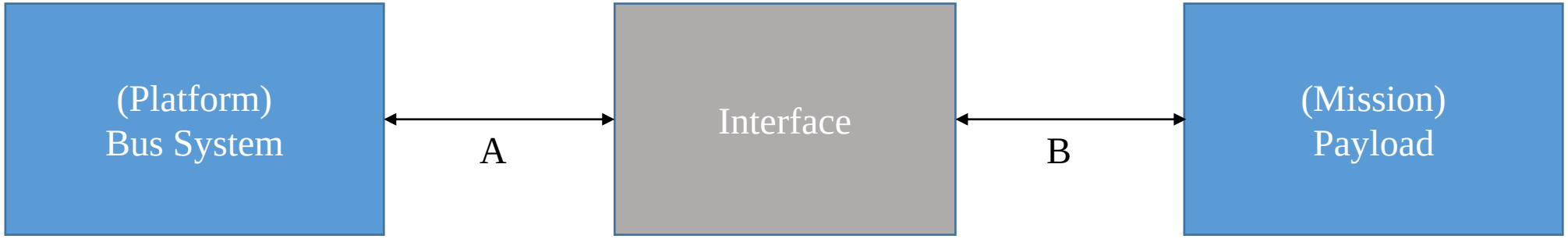
Cho, M., et al., CubeSat Electrical Interface Standardization for Faster Delivery and More Mission Success, Small Satellite Conference 2020

- ❑ Routing between system bus and mission payload is done by re-programming CPLD.
- ❑ Digital communication between bus and payload are the same.
- ❑ Digital communication is limited to UART and SPI.

Goal

To design a CubeSat interface that is

- able to route digital connections between platform (bus) and mission payload
- capable of handling communication protocols needed by satellite developers
- capable to bridge platform (bus) and mission payload which use different communication protocol



*A and B are communication protocols

Design Concept

MachXO – Interface Bridging

MachXO family of non-volatile, infinitely reconfigurable PLDs designed for applications traditionally implemented using CPLDs or low-capacity FPGAs.

MachXO2 – Flexible Interface Bridging FPGA

MachXO2 FPGA device for quickly implementing system control functions for routers, base stations, servers, storage, industrial and medical applications.

MachXO

Lattice Semiconductor Corporation

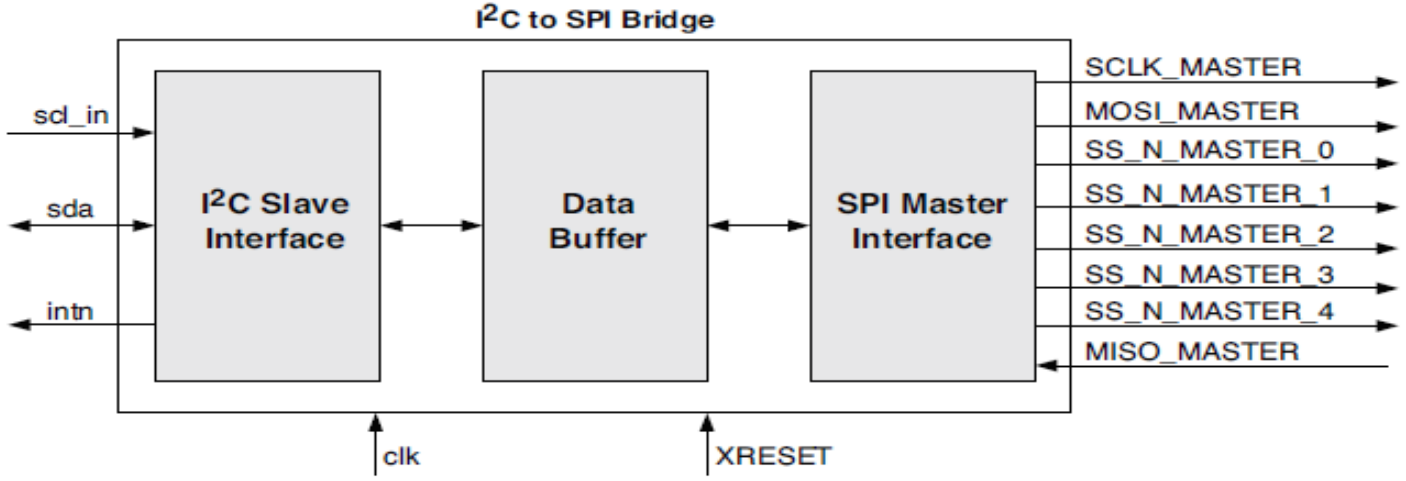
I²C Slave to SPI Master Bridge

December 2010 **Reference Design RD1094**

Introduction

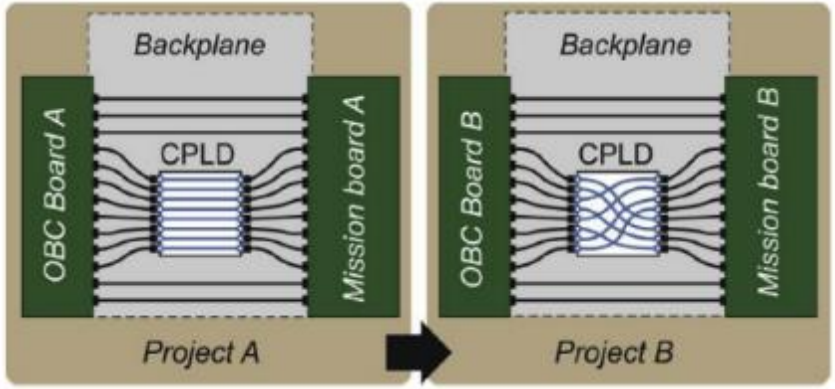
I²C and SPI are the two widely-used bus protocols in today's embedded systems. The I²C bus has a minimum pin count requirement and therefore a smaller footprint on the board. The SPI bus provides a synchronized serial link with performance in MHz range. As embedded systems are required to support an increasing number of protocols and interfaces, bridge designs targeting popular protocols provide solutions to reduce development time and cost.

This reference design implements an I²C slave to SPI master bridge. It serves as an interface between the standard I²C bus of a microcontroller and a SPI bus. This allows the microcontroller to communicate directly with the SPI bus through its I²C bus.

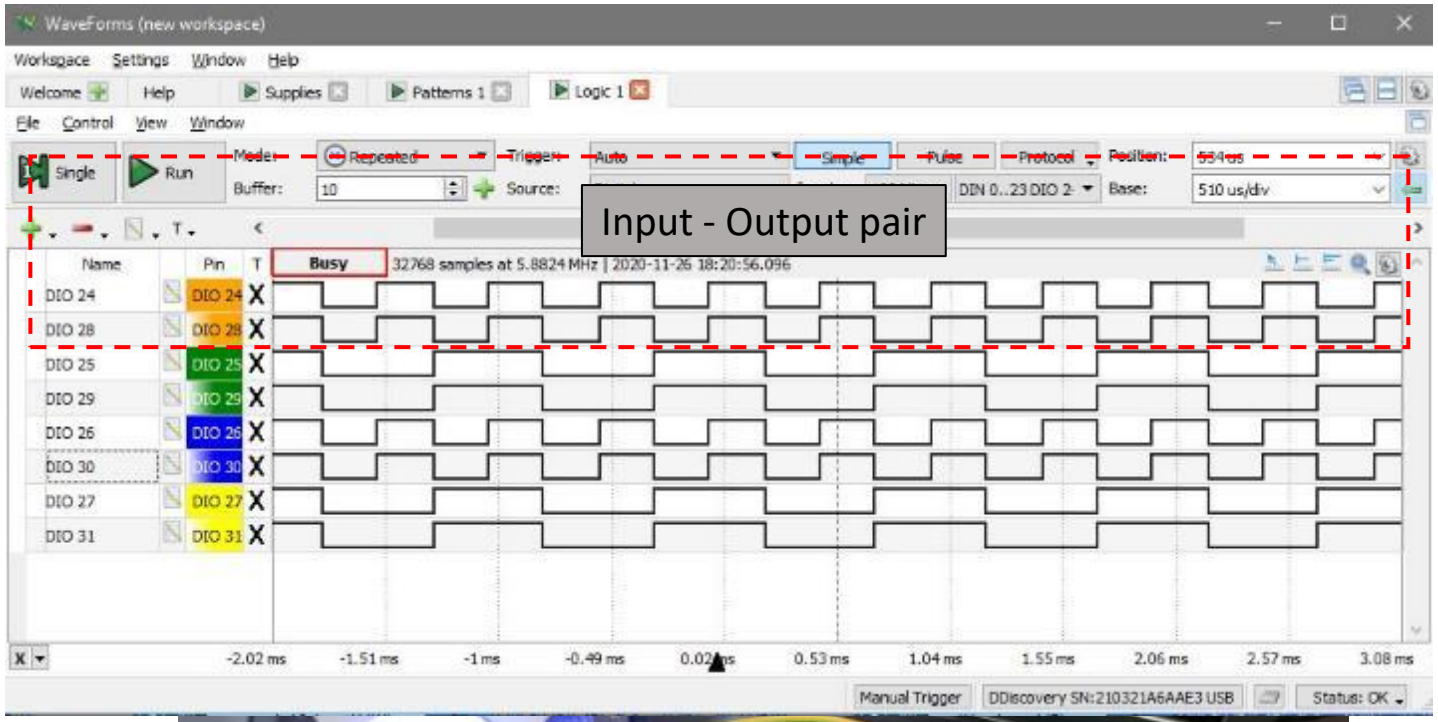


http://www.latticesemi.com/

Design Concept



Tumenjargal, T., Kim, S., Masui, H., Cho, M., CubeSat bus interface with Complex Programmable Logic Device, Acta Astronautica Vol. 160, 2019, pp. 331-342



- FPGA can replace CPLD to work as signal follower, and a bridge.