Programmable Interface Board for Higher CubeSat Form Factor and Complex Mission Payload

2021 CUBESAT DEVELOPERS WORKSHOP

Marloun Sejera*, Takashi Yamauchi, Yukihsa Otani, Mengu Cho
La SEINE, Kyushu Institute of Technology (Kyutech), Japan
Kyutech BIRDS Project

- Acronym for Joint Global Multi-Nation BIRDS Satellite Project
- Targets non-space fairing countries
- Build, test, launch and operate 1U CubeSats in two years

BIRDS-1
Japan
Ghana*
Mongolia*
Nigeria
Bangladesh*

BIRDS-2
Japan
Bhutan*
Malaysia

BIRDS-3
Japan
Nepal*
Sri Lanka*

BIRDS-4
Japan
Paraguay*
Philippines

BIRDS-5
Japan
Uganda*
Zimbabwe*

*country’s first satellite
BIRDS Standard Bus System

Implemented backplane approach
- reduce use of harness
- smaller connectors
- easy to integrate and disassemble

BIRDS CubeSat internal view
BIRDS Configurable Backplane

- 6x 50-pin board connectors (C101-C106)
- 4x 2-pin deployment switch connectors (SW1-SW4)
- 5x 12-pin panel connectors (SP1-SP5)
- 1x JTAG for CPLD programming
Routing between system bus and mission payload is done by re-programming CPLD.
Moving up

- More launch opportunities on bigger CubeSats
- Need to demonstrate the scalability of programmable interface board

Source: https://www.nanosats.eu/img/fig/Nanosats_years_types_2021-01-01.png
6U CubeSat

- 3 sections: 3U Camera payload, 1U payload, and 2U main bus
- Sections are inter-connected through backplane
6U CubeSat Backplane

- 12x 50-pin board connectors (6x main bus + 6x payload)
- 6x 4-pin board connectors
- 3x 2-pin deployment switch connectors
- 3x panel connectors (2x 12-pin, 1x 25-pin)
- 2x JTAG for CPLD programming
- 22 pairs of connections (UART, SPI and DIO) routed through main bus CPLD
- 1u payload has its dedicated CPLD for routing digital signals
CPLD code and verification

- Voltage/Signal follower using VHDL code.
- Input-output signal pair was verified using logic analyzer.
Thermal vacuum test

- Worst hot: +60°C
- Worst cold: -15°C
- Cycles: 2
Vibration Test

Random Vibration QT Profile

<table>
<thead>
<tr>
<th>Envelope (QT)</th>
<th>Freq. (Hz)</th>
<th>PSD (g2/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a) -Z axis</td>
<td>20</td>
<td>0.04</td>
</tr>
<tr>
<td>(b) +Z axis</td>
<td>50</td>
<td>0.04</td>
</tr>
<tr>
<td>(c) +Y axis</td>
<td>120</td>
<td>0.062</td>
</tr>
<tr>
<td>(a) -Z axis</td>
<td>230</td>
<td>0.062</td>
</tr>
<tr>
<td>(b) +Z axis</td>
<td>1000</td>
<td>0.009</td>
</tr>
<tr>
<td>(c) +Y axis</td>
<td>2000</td>
<td>0.0026</td>
</tr>
<tr>
<td>Overall (Grms)</td>
<td>5.77</td>
<td></td>
</tr>
<tr>
<td>Duration (s)</td>
<td>120</td>
<td></td>
</tr>
</tbody>
</table>

Sine Burst Vibration QT

| SINE BURST QT |
|---------------|-------------|-------------|-------------|
| Direction     | Freq. [Hz]  | QT          |
|               | Number of waves | Acceleration [G] |
| Vertical axis (Y) | 10~40   | 10 or more  | 11.25       |
| Horizontal axis (X, Z) | 10~40 | 10 or more  | 11.25       |

(a) -Z axis- Front view  (b) +Z axis Back view  (c) +Y axis- Top view
Summary

- A backplane was designed to demonstrate the scalability of programmable interface board.
- It is used in a 6U CubeSat which houses a 3U camera payload, 2U main bus and a 1U payload.
- Complex programmable logic device (CPLD) ICs were used to route digital lines within the backplane. CPLD has flight heritage from BIRDS project.
- The satellite passed space environment tests (i.e. TVT and vibration test)
- The satellite is targeted to launch by end of the year.
Platform-payload interface

BIRDS-3 Standard Bus system → CPLD* → BIRDS-3 mission payload (Camera, ADC, LDM)

*Complex Programmable Logic Device
Routing between system bus and mission payload is done by re-programming CPLD.
Digital communication between bus and payload are the same.
Digital communication is limited to UART and SPI.
Goal

To design a CubeSat interface that is
- able to route digital connections between platform (bus) and mission payload
- capable of handling communication protocols needed by satellite developers
- capable to bridge platform (bus) and mission payload which use different communication protocol

*(A and B are communication protocols)*
Design Concept

MachXO – Interface Bridging
MachXO family of non-volatile, infinitely reconfigurable PLDs designed for applications traditionally implemented using CPLDs or low-capacity FPGAs.

MachXO2 – Flexible Interface Bridging FPGA
MachXO2 FPGA device for quickly implementing system control functions for routers, base stations, servers, storage, industrial and medical applications.

http://www.latticesemi.com/
FPGA can replace CPLD to work as signal follower, and a bridge.