



# Cost-effective rad-hard MCU Solution for SmallSats

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## VORAGO Technologies

- Privately held fabless semiconductor company headquartered in Austin, TX
- Patented HARDSIL<sup>®</sup> foundation technology
- Focussed on space technology since 2004. Commercializing technology since 2015

VORAGO Technologies, Austin, Texas.



## HARDSIL<sup>®</sup> - Technology

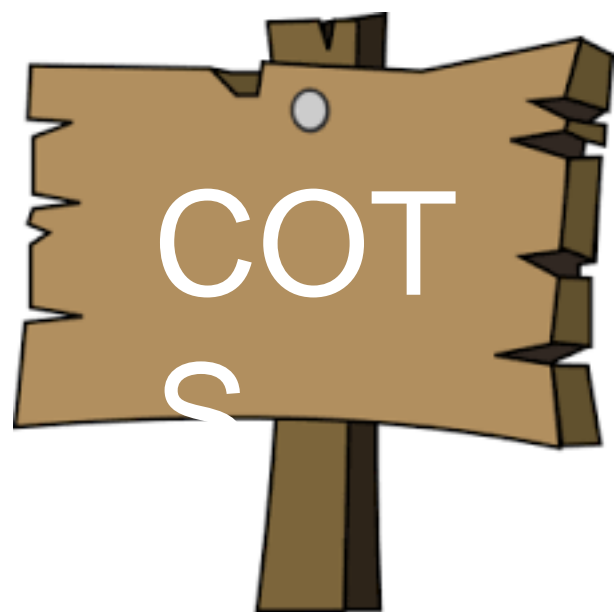
- Patented semiconductor technology (13 patents to date)
- Licensed to LSI, TI and Global Foundries
- Embedded into standard CMOS manufacturing process
  - Standard manufacturing equipment
  - Fully design agnostic
  - Enhances EOS/ESD performance
  - Eliminates latch-up
  - Improves noise floor immunity
  - Enables high temperature performance beyond 200°C
- Hardens silicon against radiation, temperature and electrical stress

## HARDSIL<sup>®</sup> - Products

- Radiation hardened portfolio up to 300k RAD
  - 8M & 16M SRAMs
  - ARM<sup>®</sup> Cortex<sup>®</sup>-M0 MCU
- High temperature portfolio 200°C
  - ARM<sup>®</sup> Cortex<sup>®</sup>-M0 MCU



## Component Options for CubeSats



- Lots of choices
- State-of-the-art
- Inexpensive
- Risky

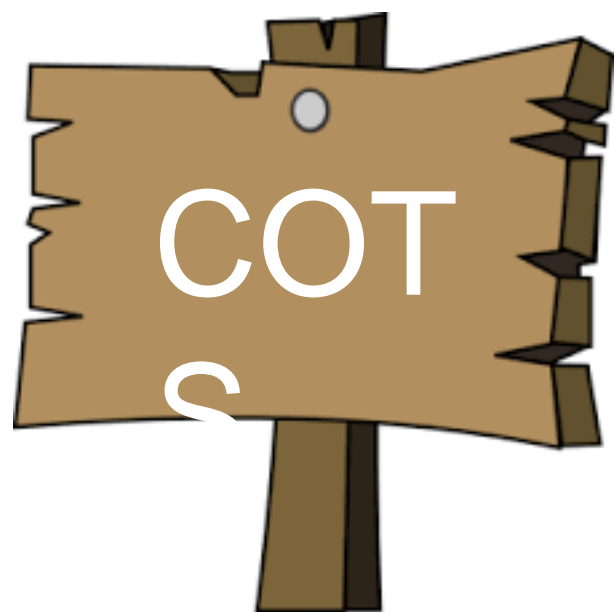


Up-screening  
is paying to  
reduce risk



- Limited choices
- Legacy art
- Expensive
- Not so risky

## Component Options for CubeSats



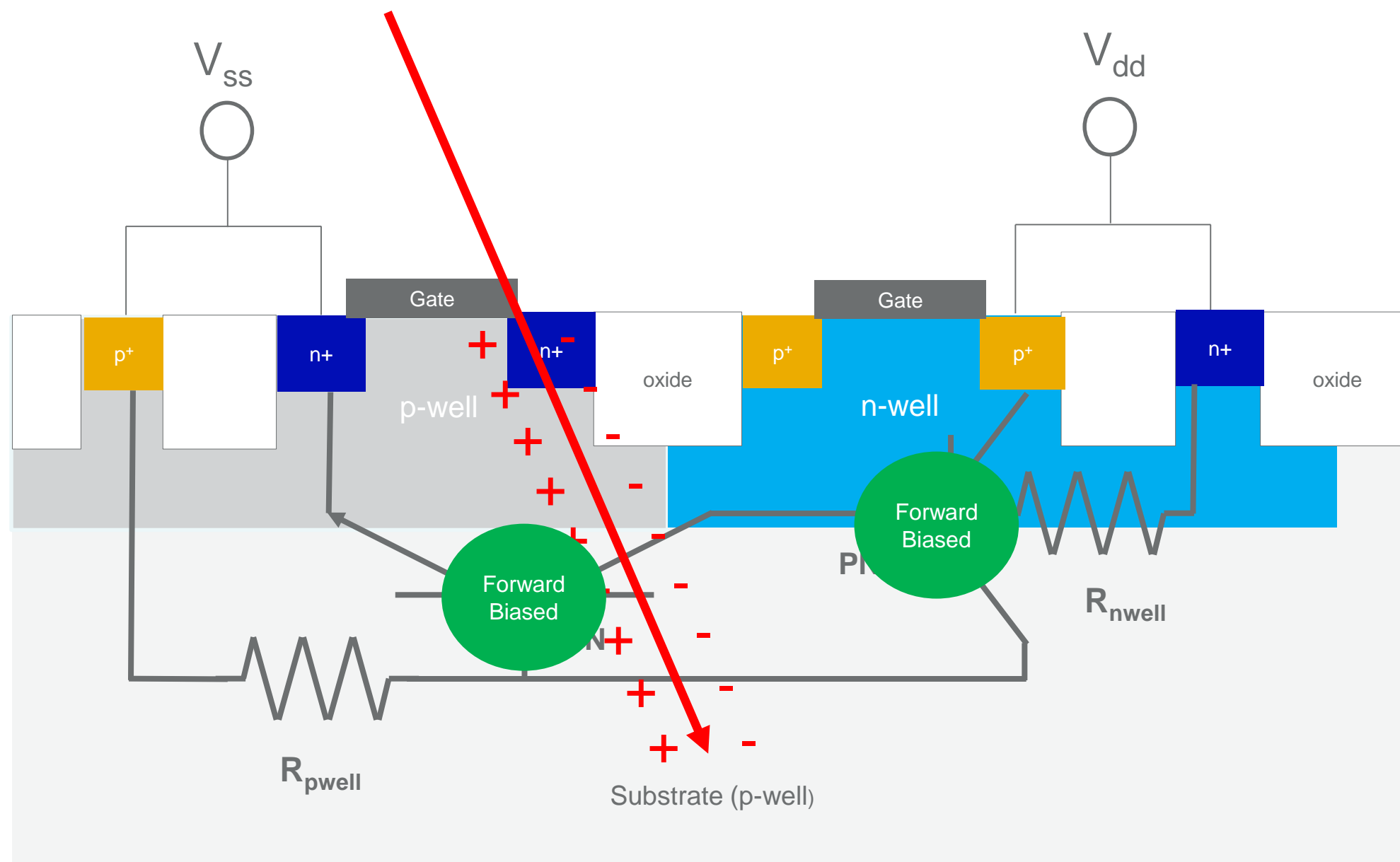
VORAGO products  
are rad-hard

## Component Options for CubeSats

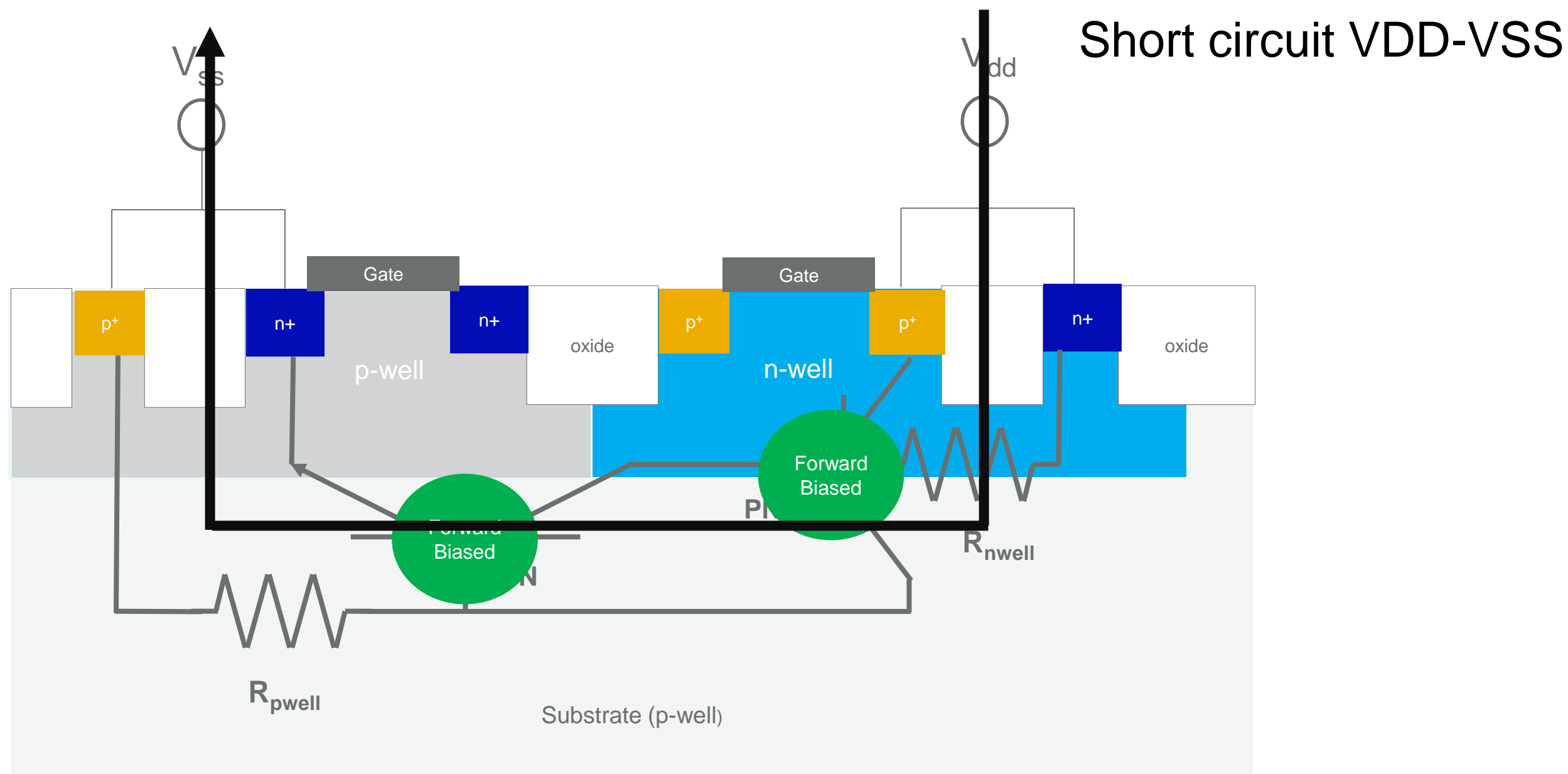


VORAGO CMOS-  
based HARDSIL<sup>®</sup>  
technology  
enables rad-hard  
solutions at a  
price lower than  
up-screening  
COTS

## What is radiation-induced latch-up ?

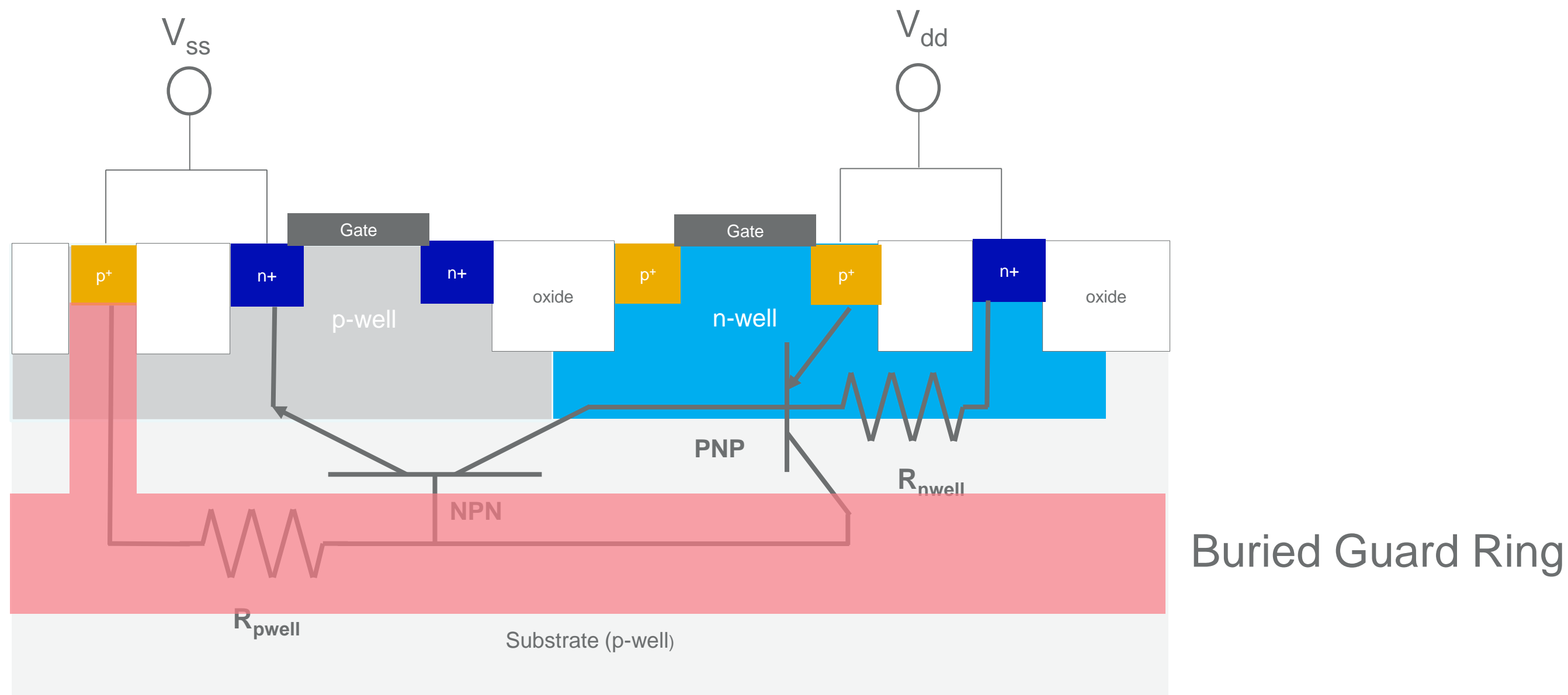


## What is radiation-induced latch-up ?





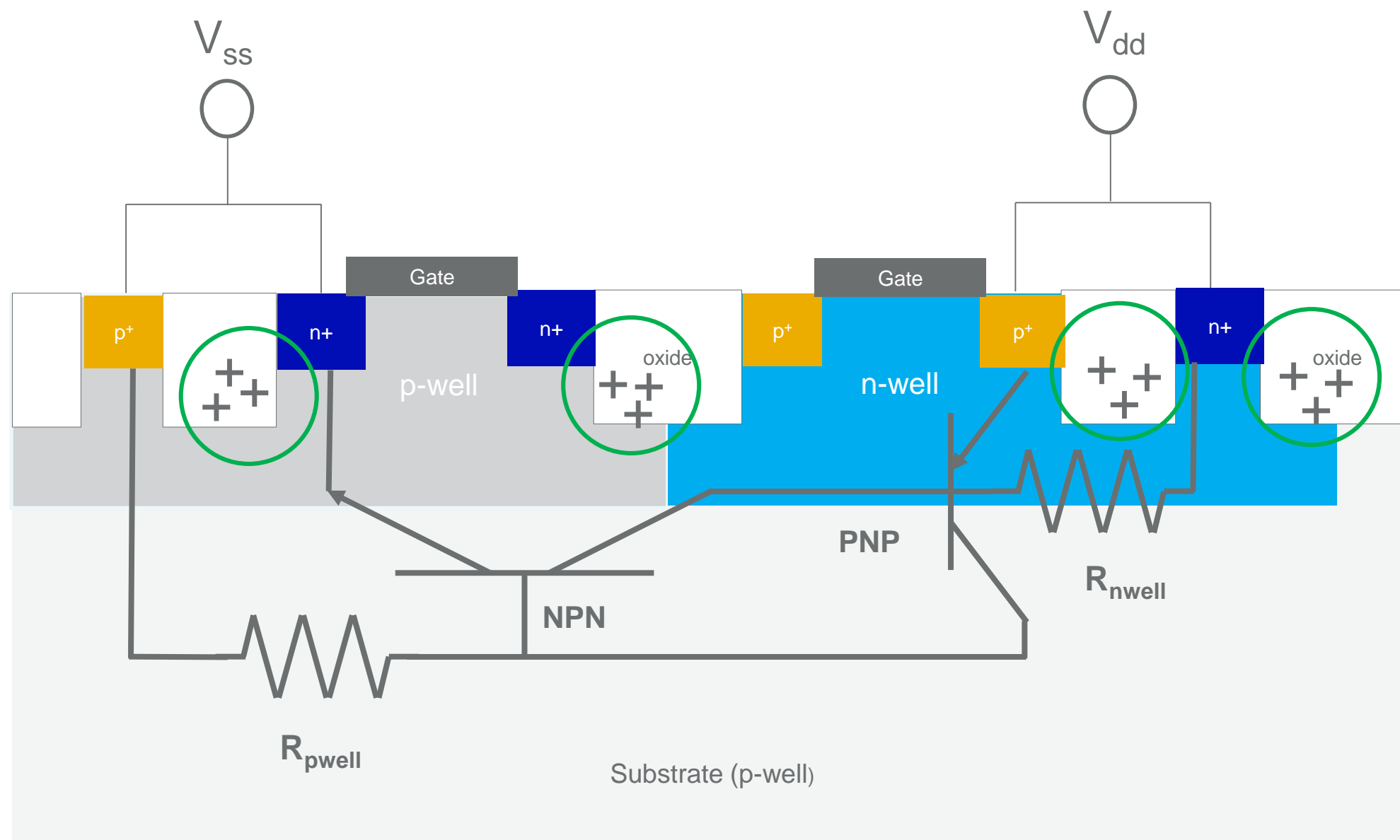
## How does HARDSIL<sup>®</sup> prevent latch-up ?



HARDSIL<sup>®</sup> creates a highly conductive layer underneath the CMOS devices and wells combined with a high conductivity connection to well contacts

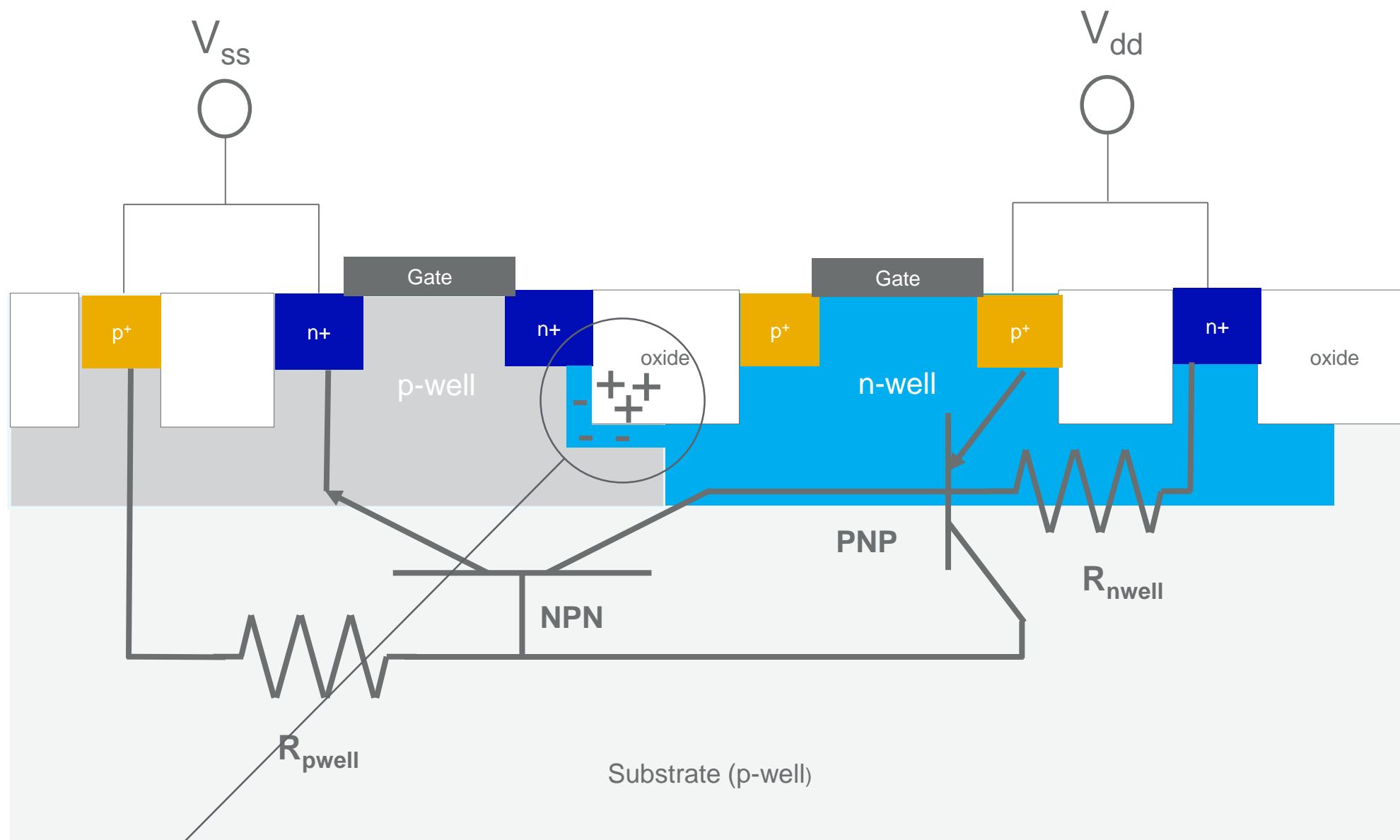


## How does Total Ionizing Dose (TID) cause my device to fail ?



Positive charge build-up in oxide regions

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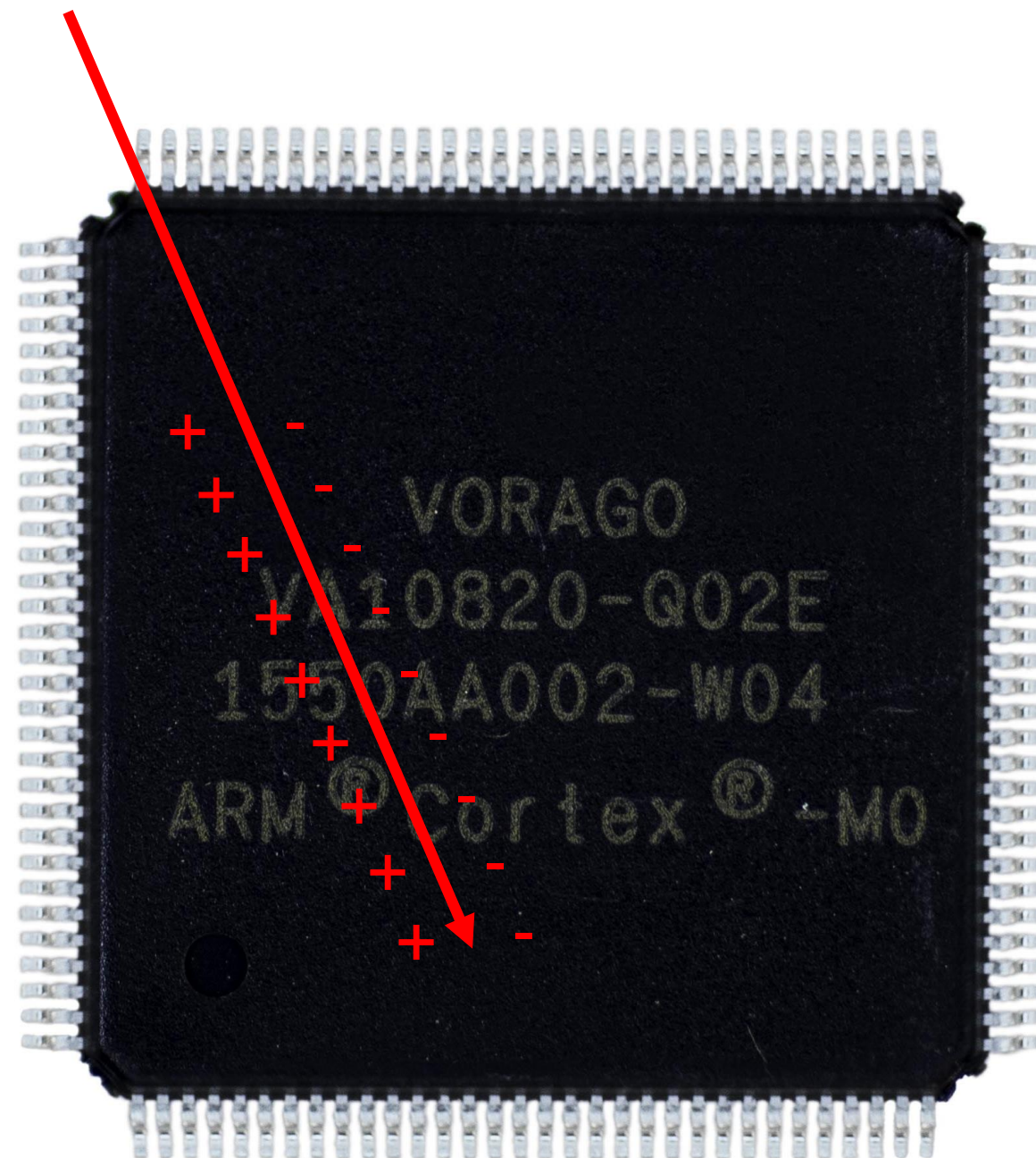


Positive charge build-up in oxide creates low resistance pathways that allow n+ to n-well leakage

## How does the VA10820 deal with Single Event Upsets ?

### SEU – Memory

- EDAC (detect 2 correct 1 bit, per byte)
- Scrub Engine – programmable rate, prevents accumulated uncorrectable errors
- Layout designed to space logically adjacent bits apart
- SER – EDAC enabled –  $1e-15$  errors / bit-day\*
- HARDSIL reduces SEEs



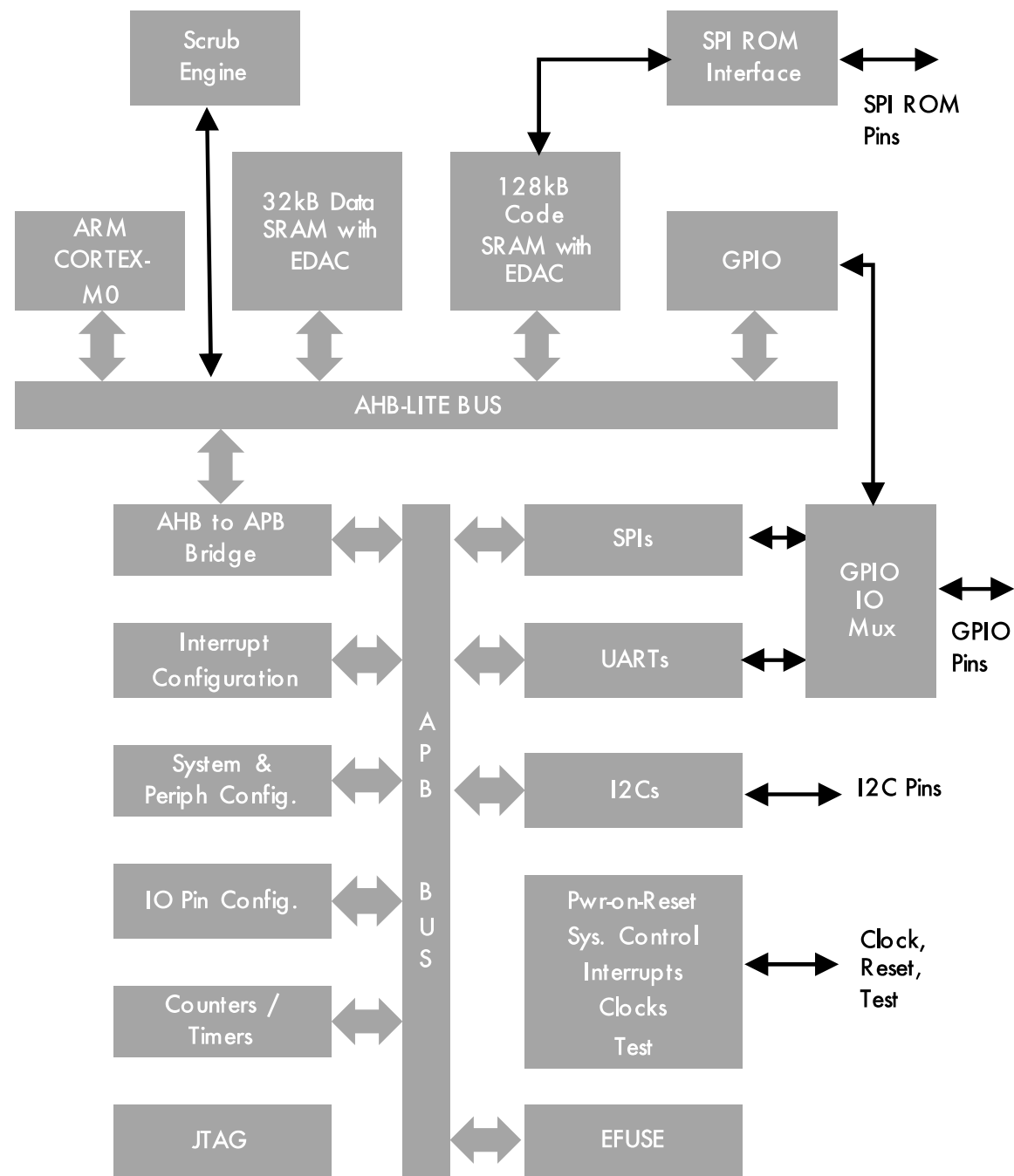
### SEU – Logic

- DICE latches
- TMR DICE latches
- All internal registers
- Clock glitch filters
- HARDSIL reduces SEEs

\* At geosynchronous solar min. with 100 mils of aluminum shielding

## VA10820

### Radiation-hardened ARM® Cortex®-M0 Microcontroller



### Key Features and Advantages

- Latch up Immune with *HARDSIL*® Hardened by Process Technology
- Power Gating and Hardware Debugger
- 32KB Data and 128KB Program Memory
- 1Kb One Time Programmable Configuration Memory (OTP)
- 24 Counter/Timers with Extensive Hardware/Software Triggering
- 3 SPI (one SPI is master only), 2 I<sup>2</sup>C, and 2 UART External Interfaces
- 56 Multiplexed General Purpose 3.3V I/O (GPIO)

### Specifications

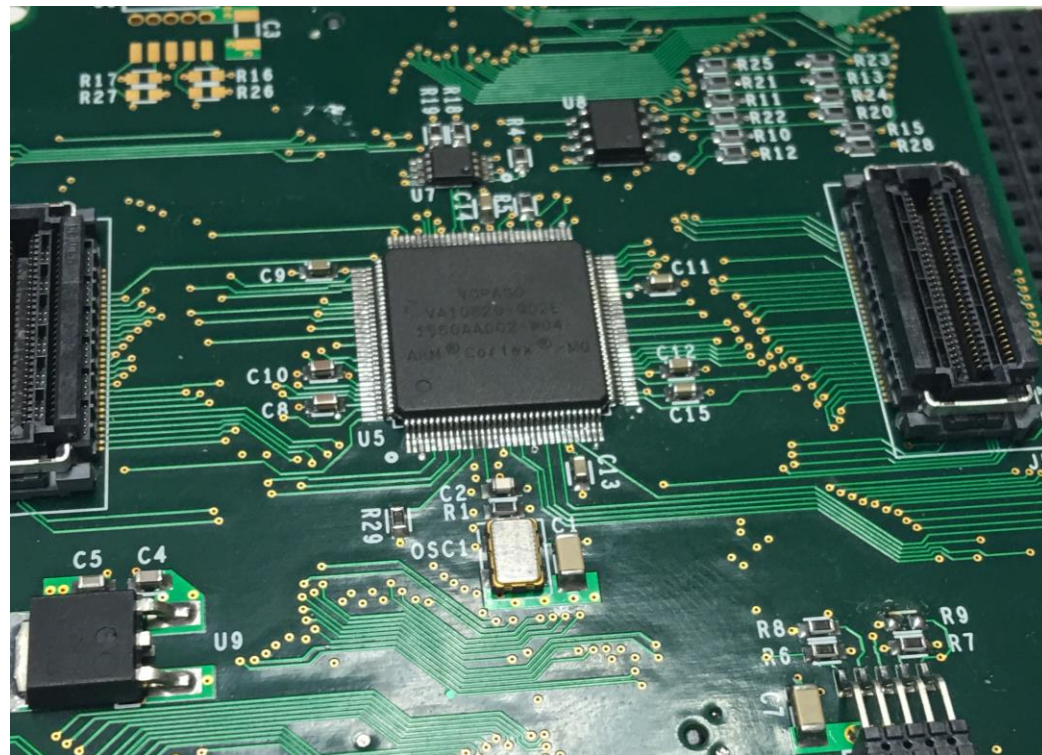
- Total Ionizing Dose (TID) – 300K rad(Si)
- Soft Error Rate (SER) with EDAC disabled – 1.3e-7 errors/bit-day
- Soft Error Rate (SER) with EDAC enabled – 1e-15 errors/bit-day
- Linear Energy Transfer (LET) – 110 MeV-cm<sup>2</sup>/mg (at T=125C)

Description	Part number	Environment	Temperature Range	Package
Radiation-hardened microcontroller	VA10820-D000F0PCA	Rad-hard 300K rad (Si)	-55 to 125°C	Die
Radiation-hardened microcontroller	VA10820-CQ128F0ECA	Rad-hard 300K rad (Si)	-55 to 125°C	Ceramic 128 LQFP
Radiation-hardened microcontroller	VA10820-PQ128F0PCA	Rad-hard 300K rad (Si)	-55 to 125°C	Plastic 128 LQFP



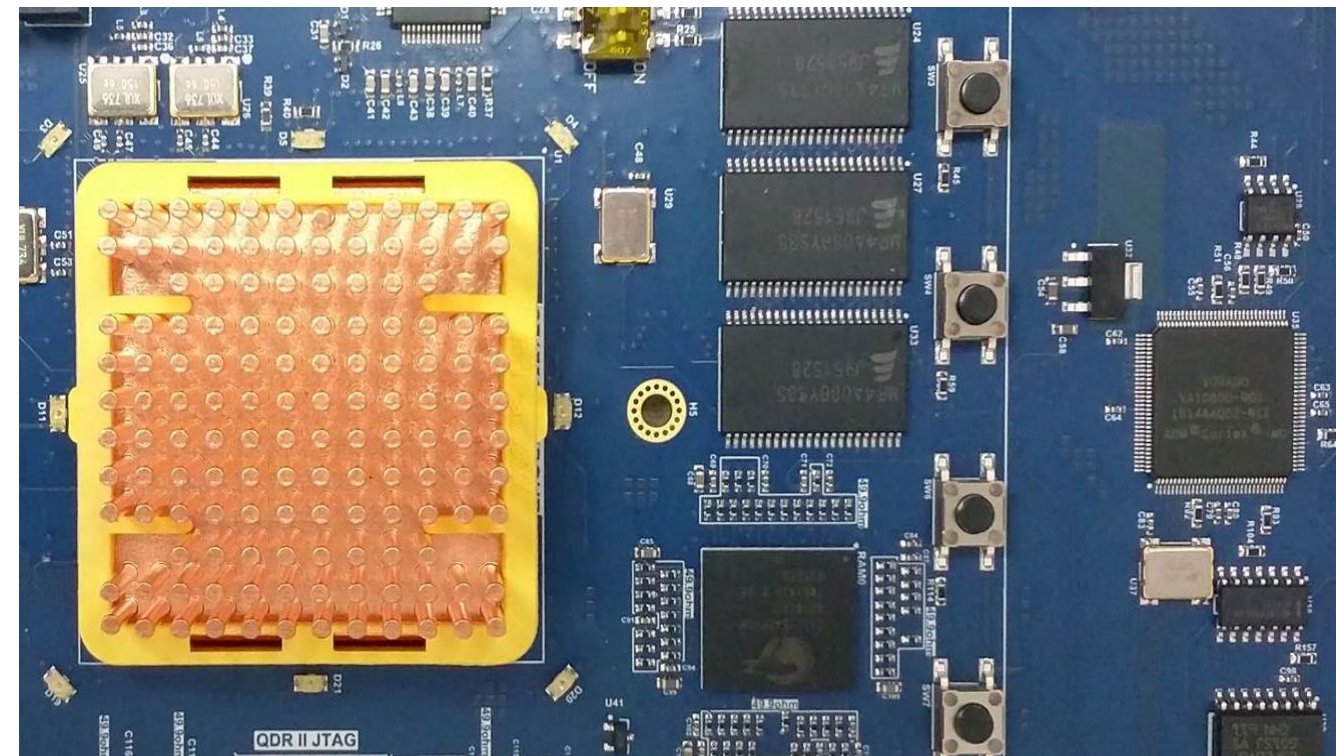
## Two Common Use-Cases for VORAGO MCUs in CubeSats Today

### Standalone OBC



- Main system controller
- Tech Brief available (Pumpkin compatible board)

### System Monitor / Watchdog



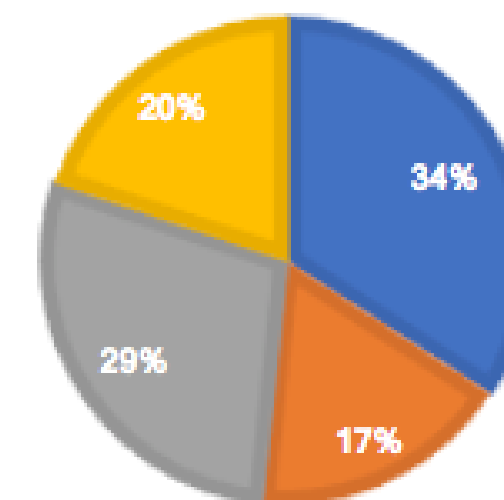
- Monitor FPGA and other subsystems
- Configuration of FPGA

## ARM® Cortex®-M0 is optimized for low power consumption

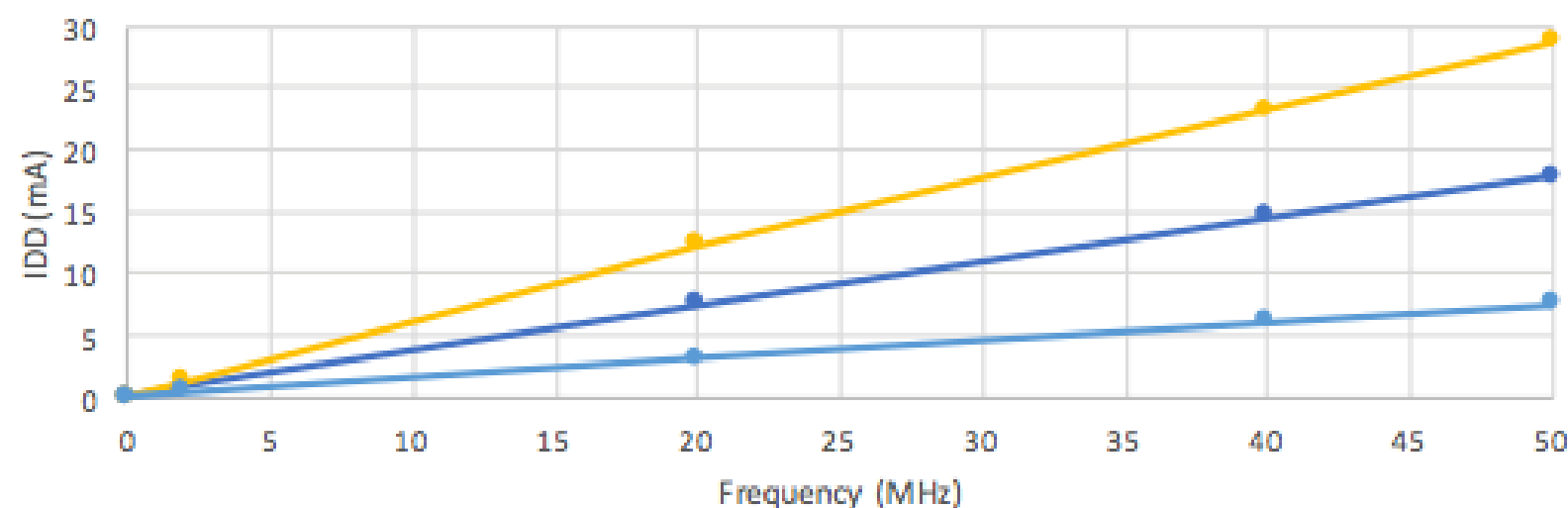
- Clock gating implemented on all peripherals
- WFI (Wait For Interrupt) instruction idles CPU
- CPU frequency can be adjusted to reduce power
- Power management Application Note available

### VA10820 MCU IDD Breakdown

- CPU + Memory Access
- Clock and always On MCU peripherals
- 24 Timers
- 2 x I2C, 3 x SPI, 2 x UART, GPIO



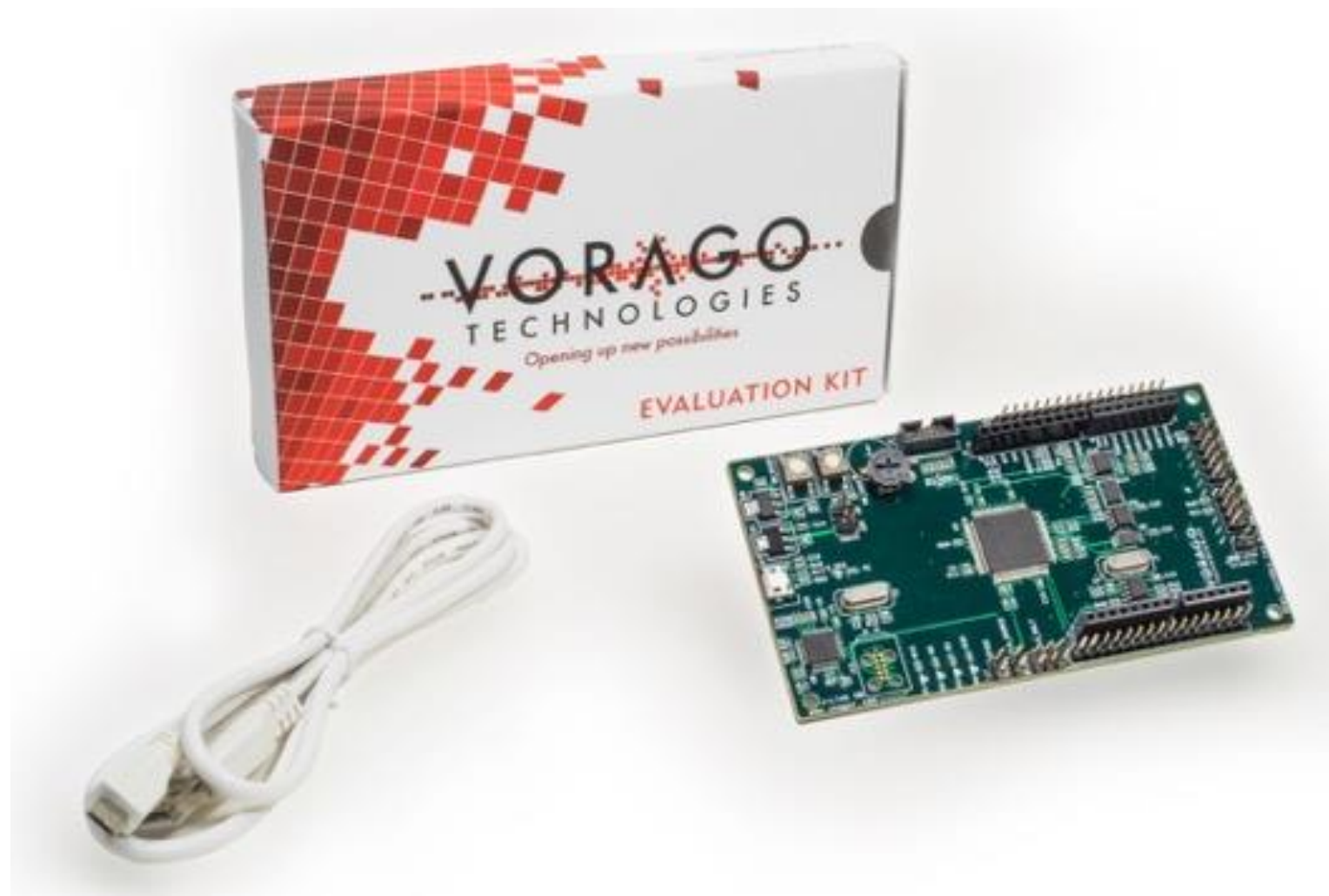
### VA10820 MCU Core IDD with Operating Frequency







- CPU Run, no peripherals on, no timers on
- CPU Run, all peripherals on, all timers on
- Sleep, no peripherals on, no timers on



## REB1-VA10820 Development Board



- Huge ecosystem of development tools
- All popular ARM compilers support VORAGO
- Board Support Package available
- Application notes available

	Supplier	Software Development Kit
	ARM Keil	MDK Microcontroller Development Kit
	IAR Systems	IAR Embedded Workbench
	iSYSTEM	winIDEA
	FreeRTOS	Real-time Operating System

The logo for VORAGO TECHNOLOGIES features the word "VORAGO" in a large, white, sans-serif font. A horizontal trail of red, pixelated squares passes through the middle of the letters. Below "VORAGO" is the word "TECHNOLOGIES" in a smaller, white, sans-serif font.

VORAGO  
TECHNOLOGIES

*Opening up new possibilities*