CubeSat Avionics Optimization

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- Introduction
- Motivation
- Approach
- Final Design
- Assessment and Discussion
- Acknowledgements

Introduction

- Candidate for S.M. in Aeronautics and Astronautics
- B.S. Aerospace Engineering with Information Technology, MIT '14
- Ensign, United States Navy
- Avionics Hardware Lead, Microwave Radiometer Technology Acceleration (MiRaTA) Spacecraft

Approach to optimizing CubeSat avionics on MiRaTA, whose mission is science technology demonstration*

***which means they keep trying to steal my SWaP*

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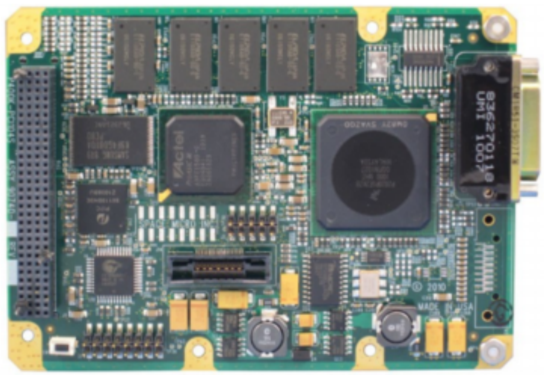
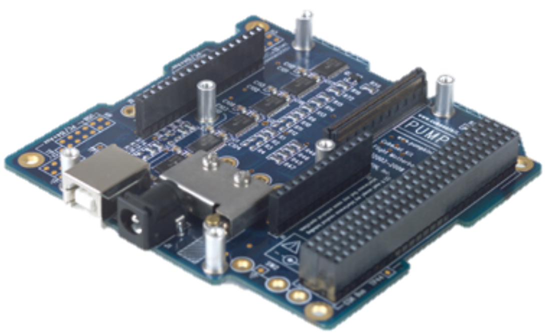
Motivation

Examples of Current State of the Art



Space Micro Proton 400K [1]

- Fits in 2U stack
- 1 GHz, dual core, 32-bit processor
- 1 MB EEPROM, 32Gb flash memory
- 8-12W operating power
- Radiation tolerance up to 100krad TID
- Support for multiple OS's (Linux, VxWorks)



Pumpkin Motherboard RevE [2]

- Fits in 1U stack
- Open architecture – up to 32MHz, 16-bit
- 256KB ROM, 64Mb flash memory
- 100mW operating power
- Tested radiation durability
- Embedded C programmable

MiRaTA needs:

Efficient management of spacecraft activities using minimal resources, with COTS parts that can survive the harsh space environment.

Motivation

Minimal Resources

Power	Size	Cost
Electrical	Volume	Money
Processing	Memory	Time

Harsh Environment

Temperature	Radiation	Vibration

MiRaTA Avionics Requirements

Requirement	Limit
Electrical Power	200 mW idle, 2 W receiving, 10 W transmitting
Processing Power	32 MHz
Volume	100 mm x 100 mm x 85 mm
Memory	2 GB storage, 256 KB program
Cost	$30,000
Time	19 months
Radiation Tolerance	9.36 krad

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Approach: Resource Management

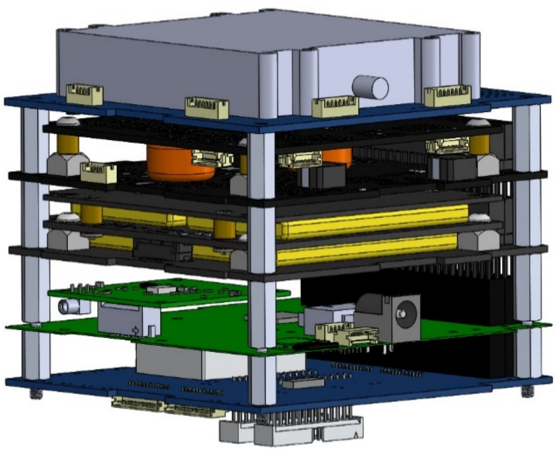
Avionics Stack

Avionics Stack
Top Interface
Electrical Power System
Batteries
Central Processing
Bottom Interface

MAXIMIZE
- Processing power
- Memory

minimize
- Electrical power
- Volume
- Cost
- Time
- Complexity

- Stacked, 4-Layer boards, no blind vias
- Smarter ICs and reprogrammability
- Off-board power/data management
- Flash memory on SPI network
- Appropriate selection of TTL vs CMOS
- **Commercial off-the-shelf (COTS) where possible**



CAD of MiRaTA avionics stack

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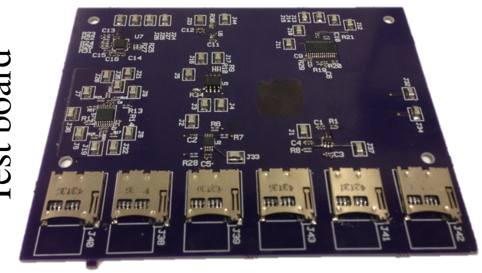
Approach: TID Radiation Testing

Expected Total Ionizing Dose for MiRaTA: 9.36 krad

*Given minimum 1mm Al shielding over 1 year mission life in SSO**

Procedure: Characterize components before and after TID gamma irradiation and compare to expected datasheet values at **8 krad**, **16 krad**, and **24 krad**

Test board



Results: Components proved suitable for proposed orbit

Gammacell 220

Component	Manufacturer	Tolerance
Industrial-Grade Micro SDs	Delkin, San Disk, Transcend	24krad
N25Q512 Serial NOR Flash Chip	Maxim	24krad
MAX892 Current Limit Switch	Maxim	24krad
FPF2000 Current Limit Switch	Fairchild	24krad
SN65HVD Line Transceiver	Texas Instruments	24krad
ADG452 SPST Switch Array	Analog Devices	16krad

*assuming an elliptical SSO

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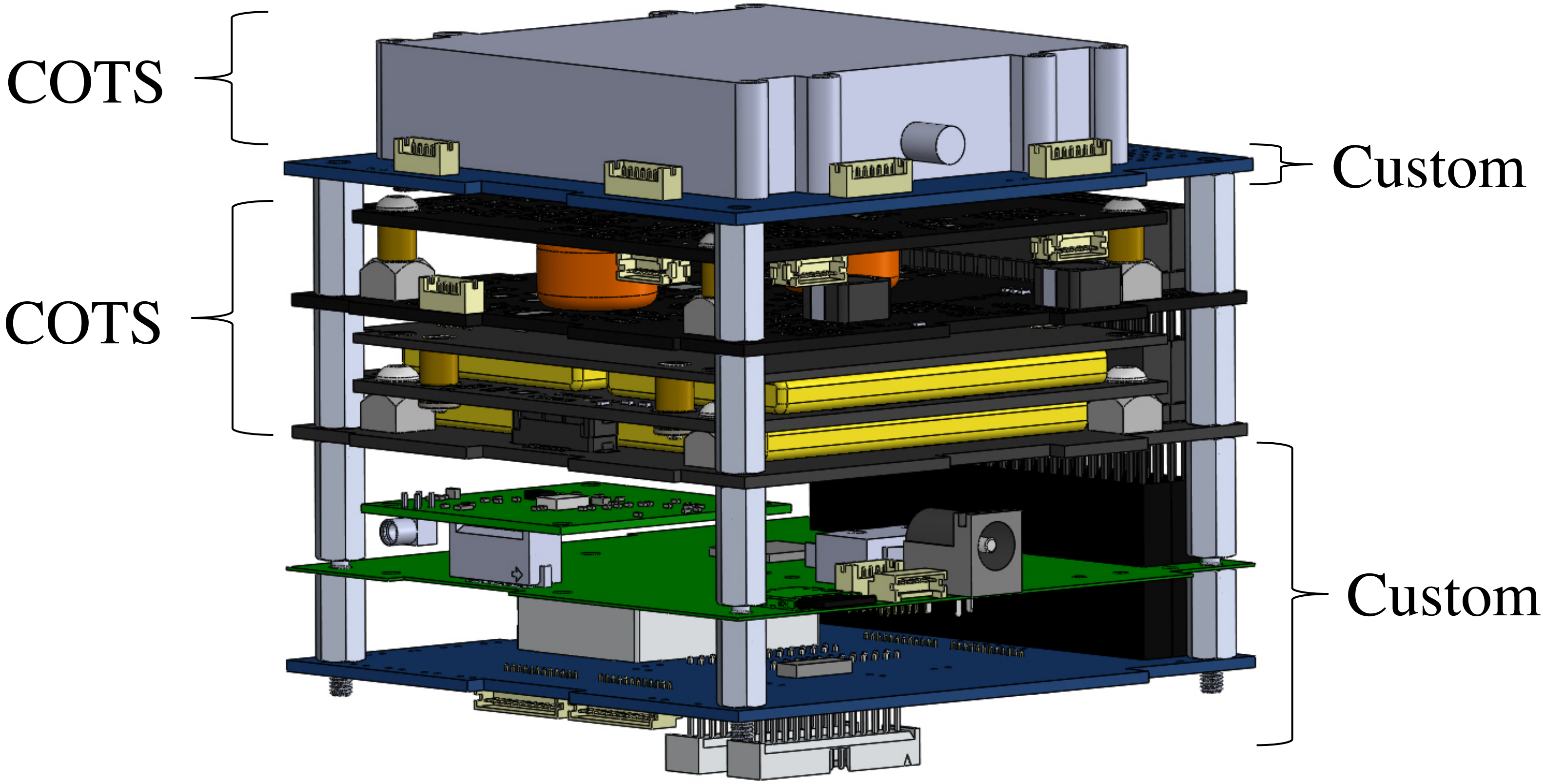
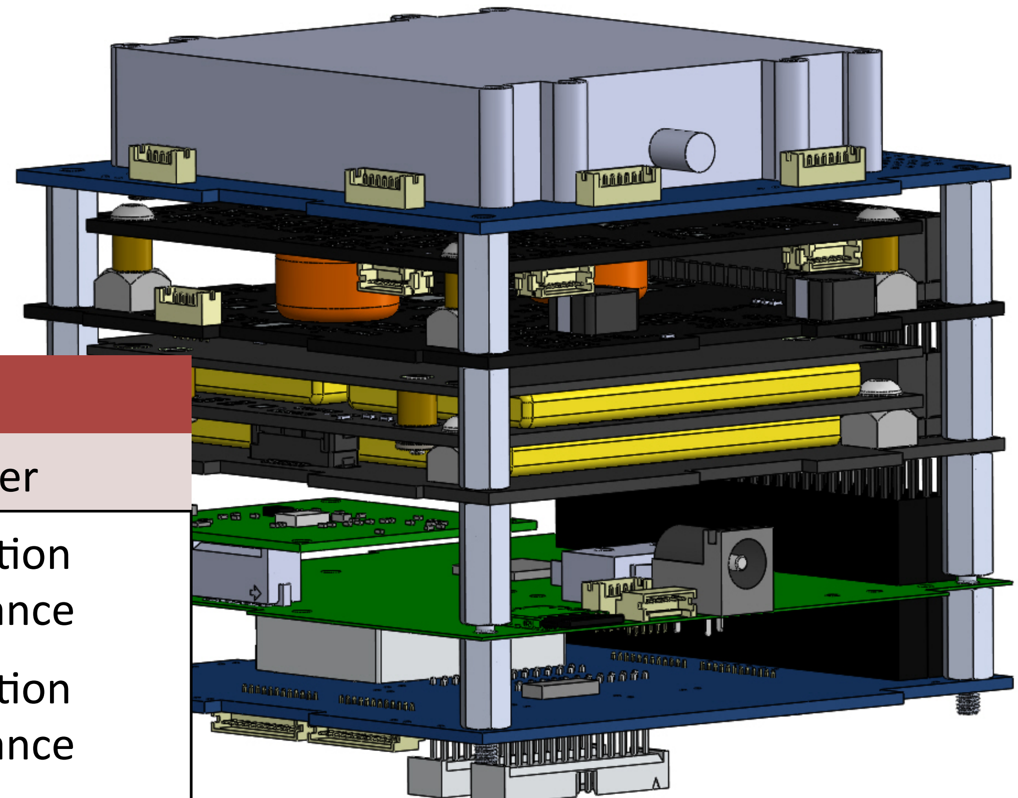
Final Design



MiRaTA Avionics Stack

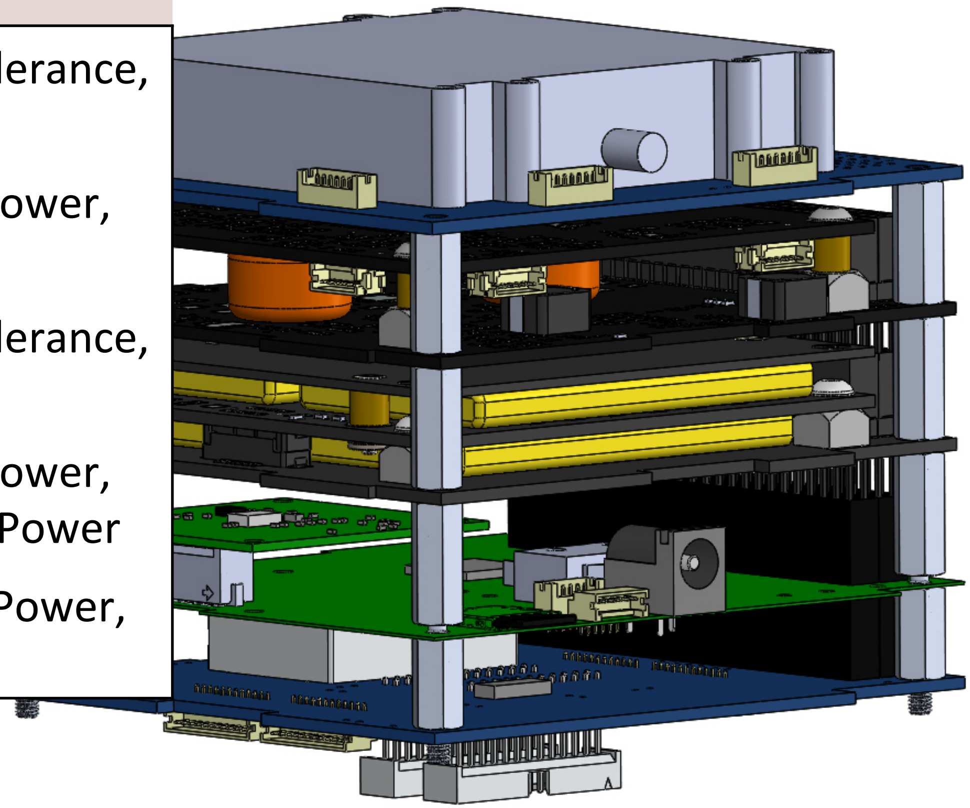
Final Design



Top Interface Board	
Sub-circuit	Driver
Payload Power Distribution	Radiation Tolerance
Payload data transceiver	Radiation Tolerance
Magnetometer	Size, Cost
Beacon Radio Interface	Electrical Power
Primary Radio	Processing Power

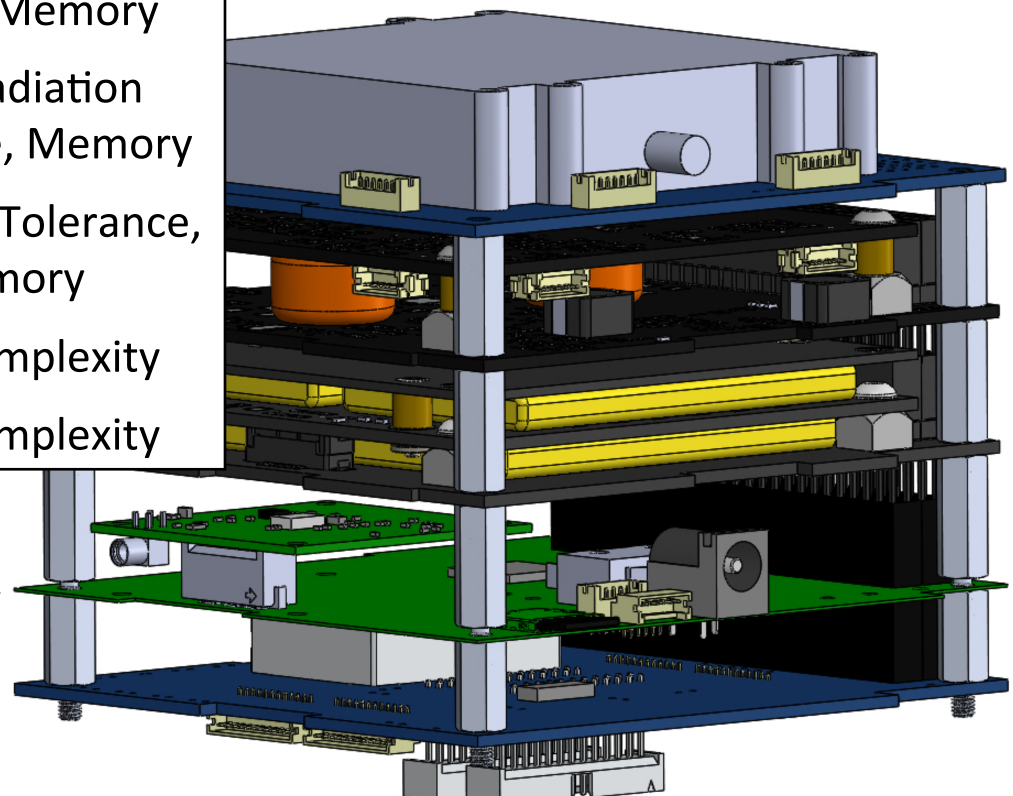
Final Design

Bottom Interface Board	
Sub-circuit	**Driver**
Temperature Compensating Crystal Oscillator	Radiation Tolerance, Time
Inertial Measurement Unit	Electrical Power, Size
Thermal Knife Drivers	Radiation Tolerance, Cost
Coarse Sun Sensors	Electrical Power, Processing Power
Resistance Temperature Detectors	Processing Power, Cost



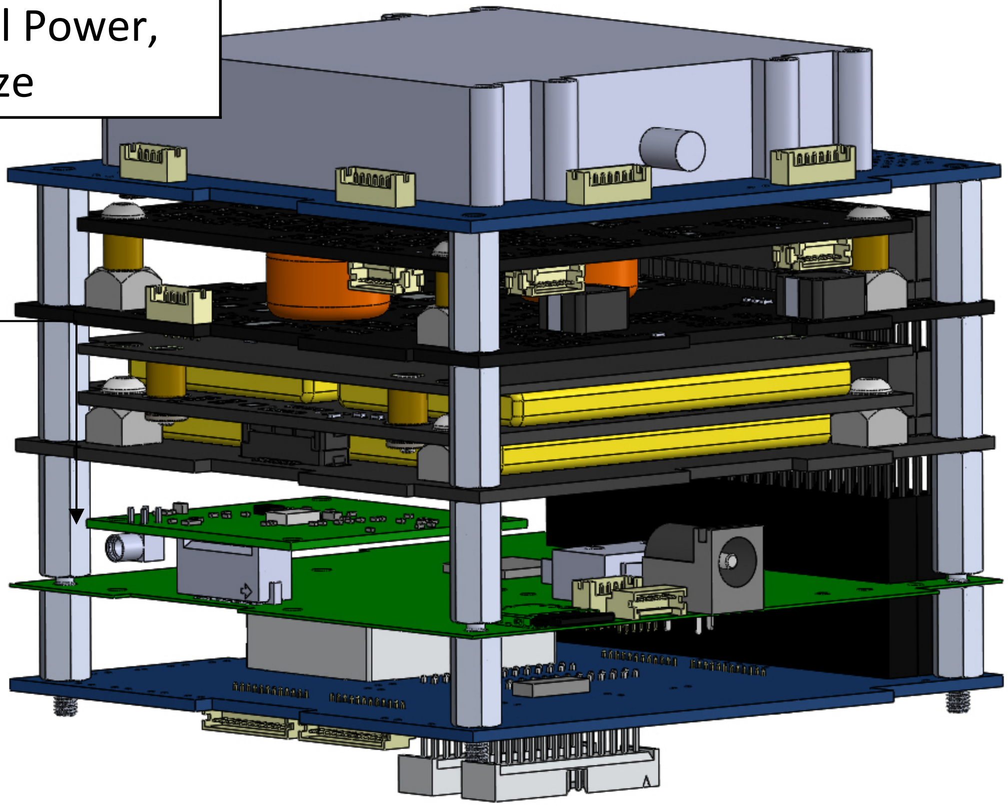
Final Design

Motherboard	
Sub-circuit	Driver
PIC24 Microcontroller	Processing Power, Cost, Electrical Power, Memory
Micro SD card	Size, Radiation Tolerance, Memory
Flash Memory	Radiation Tolerance, Memory
Serial UART interface	Size, Complexity
Unregulated Power Port	Size, Complexity

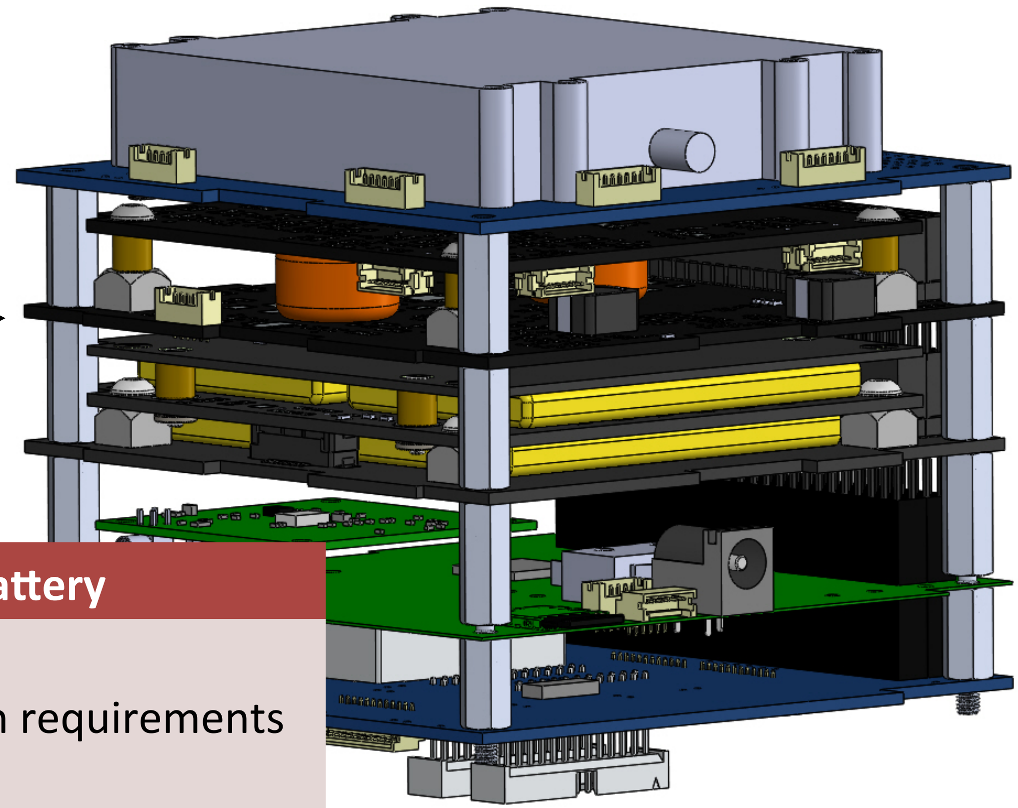


Final Design

Backup Radio	
Sub-circuit	Driver
CC1110 System-on-Chip	Processing Power, Size, Complexity
RF6504 Front End Module	Electrical Power, Size



Final Design



Electrical Power System / Battery

- Highest single-cost component
- Smallest batteries still within mission requirements (20 Whr)
- Small size
- Self-regulated processing and telemetry

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Assessment

- Processing power sufficient for the needs of the mission
- Non-volatile memory sufficient to store 2 days of science data
  - 32x more memory than Pumpkin, 32x less memory than Proton
- Size Reduction
  - Decrease from 100-200cm^2 to 70cm^2 motherboard + 30cm^2 backup radio
- Complexity minimization
  - Component reduction from Proton design by ~200%
  - Component reduction from Pumpkin design by ~50%
- Decrease in number of boards
  - From 6 in MicroMAS to 5 on MiRaTA
- Maintained power draw
  - Expected minimal decrease as compared to Pumpkin design
- Environmental durability
  - Tests indicate at least 24krad TID tolerance

Discussion

- Trade-off between size reduction, accessibility, and cost
  - If we use all 0201 components, last-minute fixes will be difficult
- Optimization will be different for each case
  - E.g., University vs industry budget, timeline, and resources
  - Hard to standardize
- Is there a "lite" avionics core that satisfies most use cases for the next 5-10 years?
  - Include common GPS, payload, sensor interfaces
  - Include some extra interfaces/capability (memory, reprogramming, better oscillators)
  - Include less common interfaces? Propulsion?
- What is the "just right" testing profile?
  - When is it better to build a bunch or sequentially, test on orbit?

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- Planet Labs
  - Henry Hallam
  - Ben Howard
- Clyde Space
- Pumpkin Inc.

References

[1] http://www.spacemicro.com/assets/datasheets/digital/slices/proton400k.pdf

[2] http://www.cubesatkit.com/docs/datasheet/DS_CSK_MB_710-00484-D.pdf

[3] http://www.nasa.gov/images/content/730041main_20130228-mona2.jpg

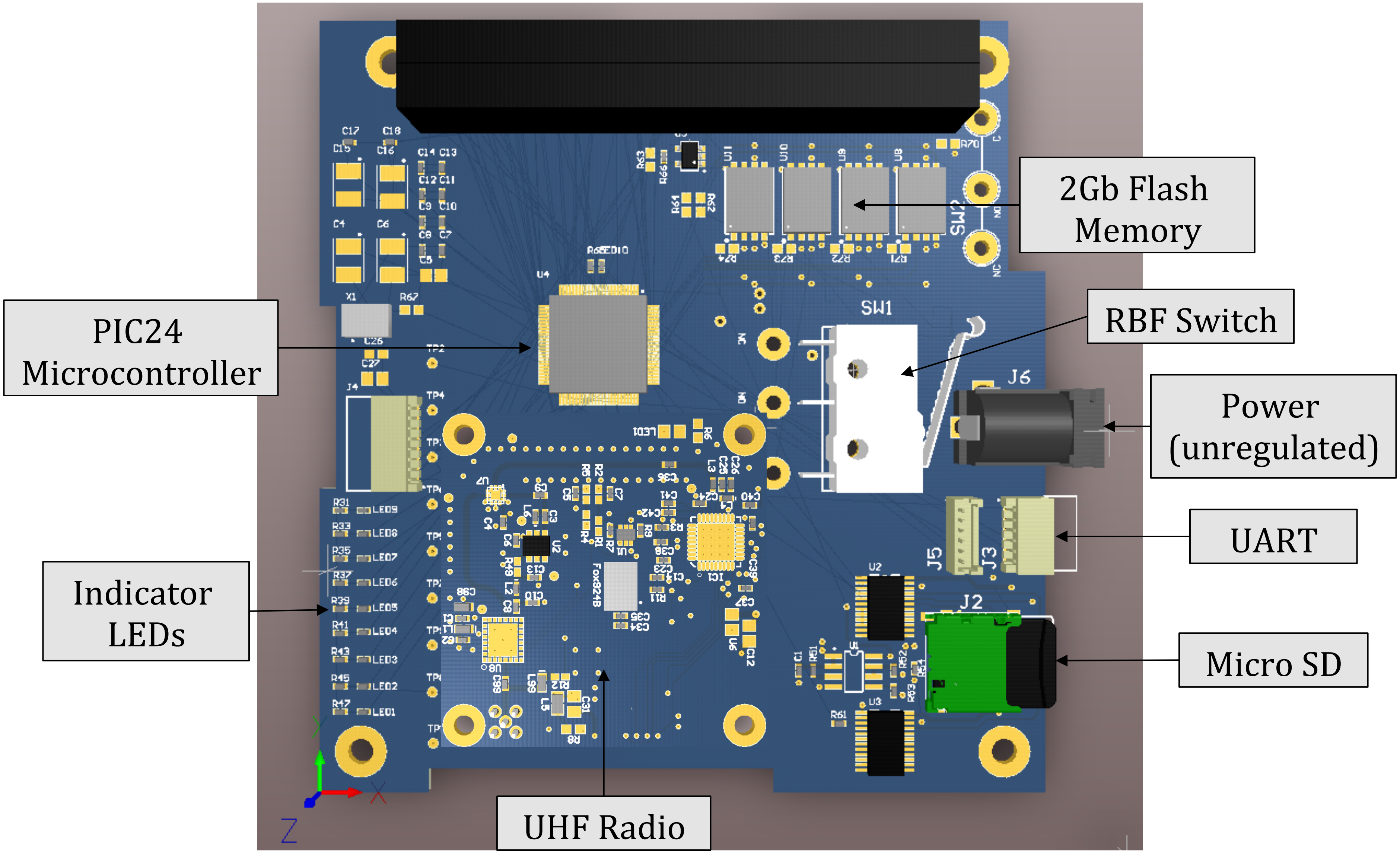
[4] http://www.silvaco.com/products/vwf/atlas/2D/rem/rem_fig3.jpg

[5] http://www.iss.infn.it/operatori

Questions?

Backup Slides

Final Design



COTS vs Custom

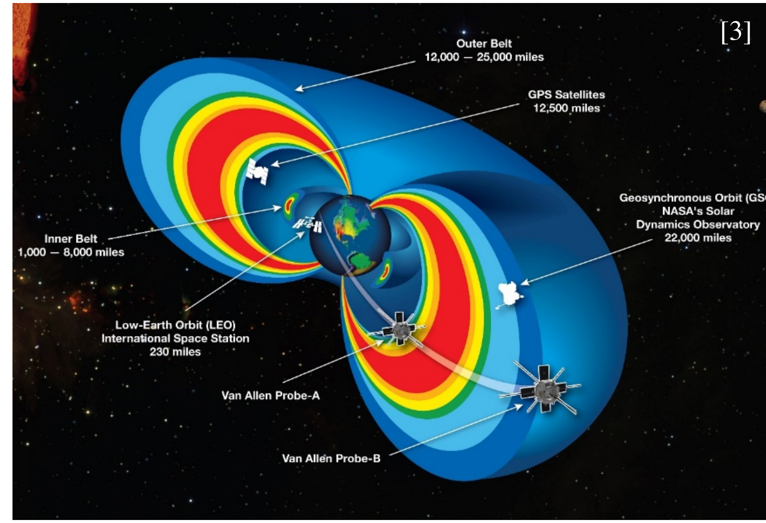
COTS	Custom
Pros • No development time • Low initial investment • User community	**Pros** • Adaptable to the mission • Full resource utilization • Structural flexibility
Cons • Unused functionality • Not designed with the future in mind • Difficult debugging	**Cons** • Higher initial investment • Some development time • May not interface with other COTS devices

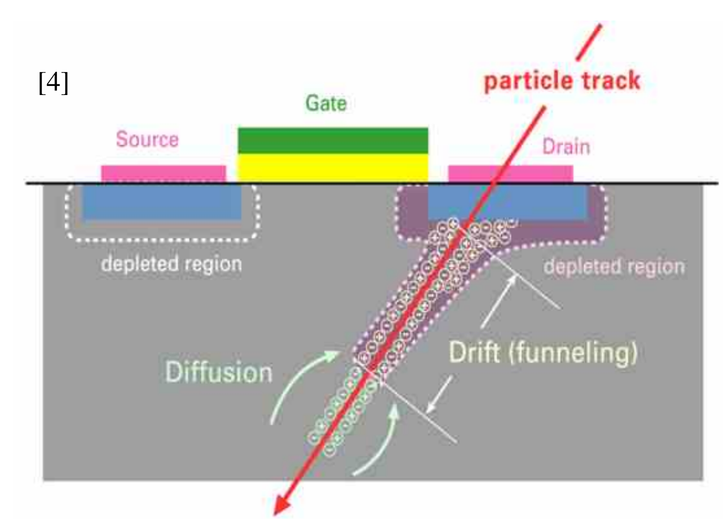
Durability: Space Radiation

Total Ionizing Dose: Long-term exposure to radiation that generates electron-hole pairs

Displacement Damage: Physical damage to materials caused by particle collisions

Single Event Effects: Unintended photoelectric events causing bit flips or other electron behavior in semiconductor logic





Design Trade-Space

	FPGA	Microcontroller
Processing Power	• Parallel execution • ~500MHz	• Real-time programmable • ~50-500MHz*
Memory	• Configurable RAM • ~1 million gates	• Internal, pre-set size • ~500kB ROM
Electrical Power	• ~50mW	• ~500mW
Volume	• 0.5U PCB to support	• 0.5U PCB to support
Cost	• ~$100 each	• ~$3 each
Time	• Significant HDL training • Lengthy development time	• Rudimentary C training • Ready off-the-shelf

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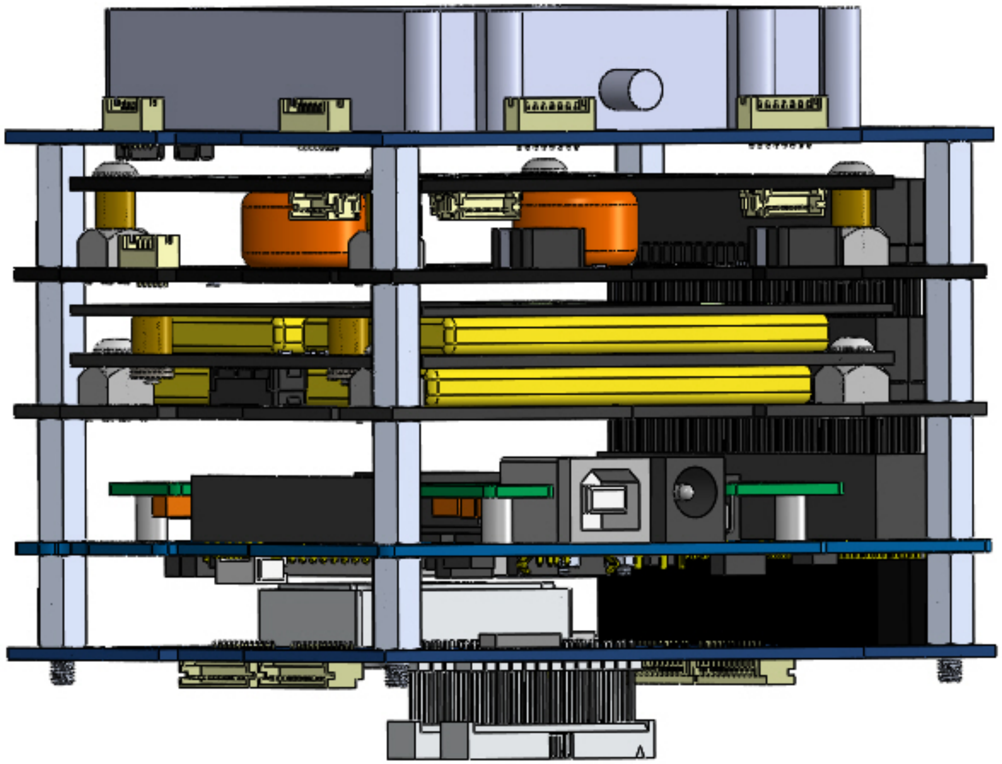
Final Design



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