A Low Power Optical Communication Instrument for Deep-Space CubeSats

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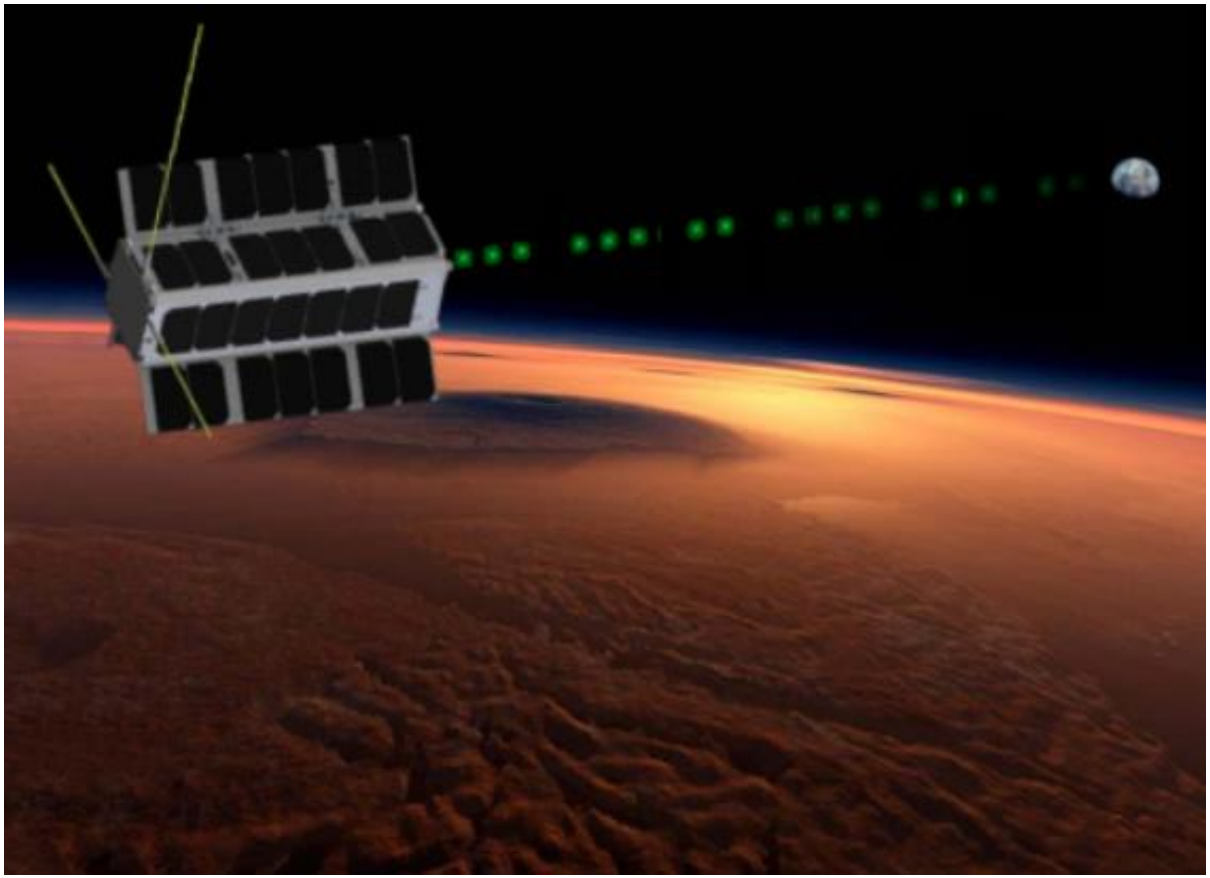


Motivation and Objectives

Objectives: Demonstrate optical communication with small volume, low power.

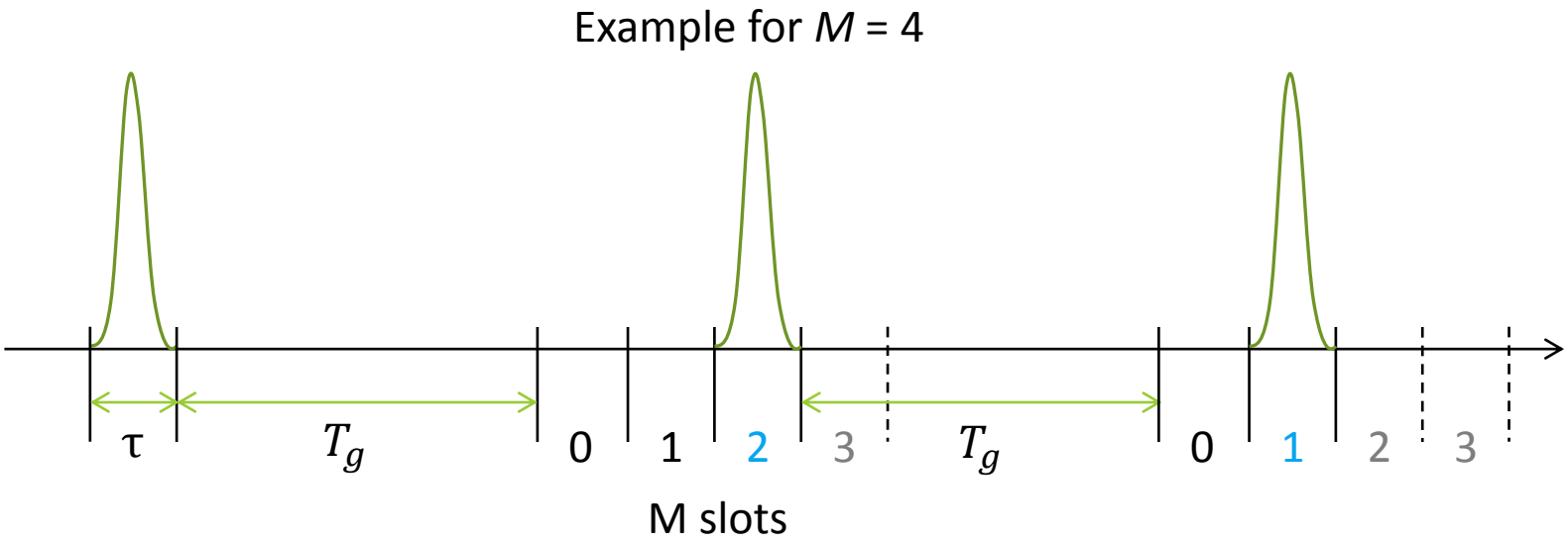
- 2U, ~5 W, 10s Mbps
- Proof of Concept (TRL 1 to TRL 3)
- Initial studies and feasibility in 2014.
- Prototype realization started in February 2015.

LLST Model on LADEE

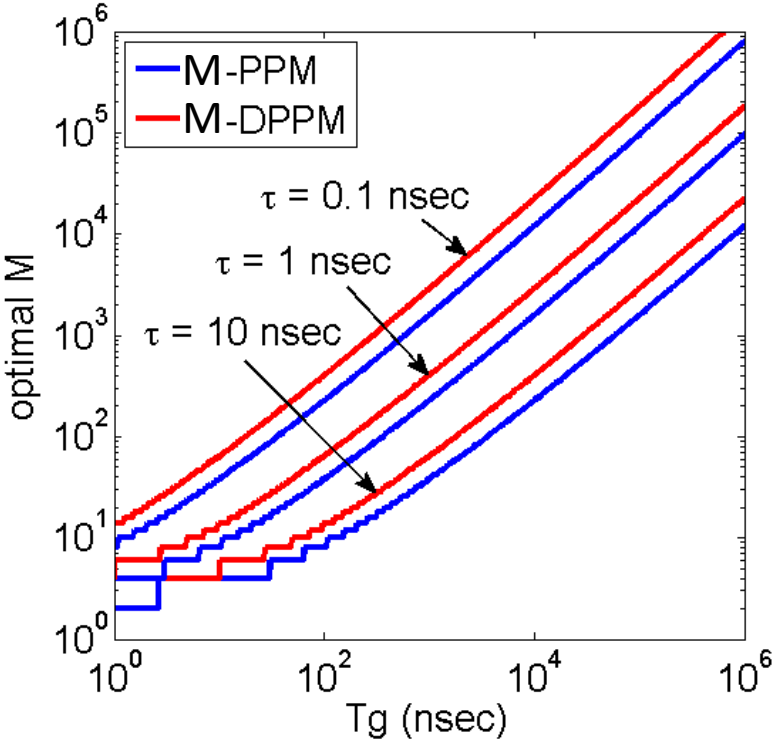
Virtex 5 QV on M-Cubed/COVE2

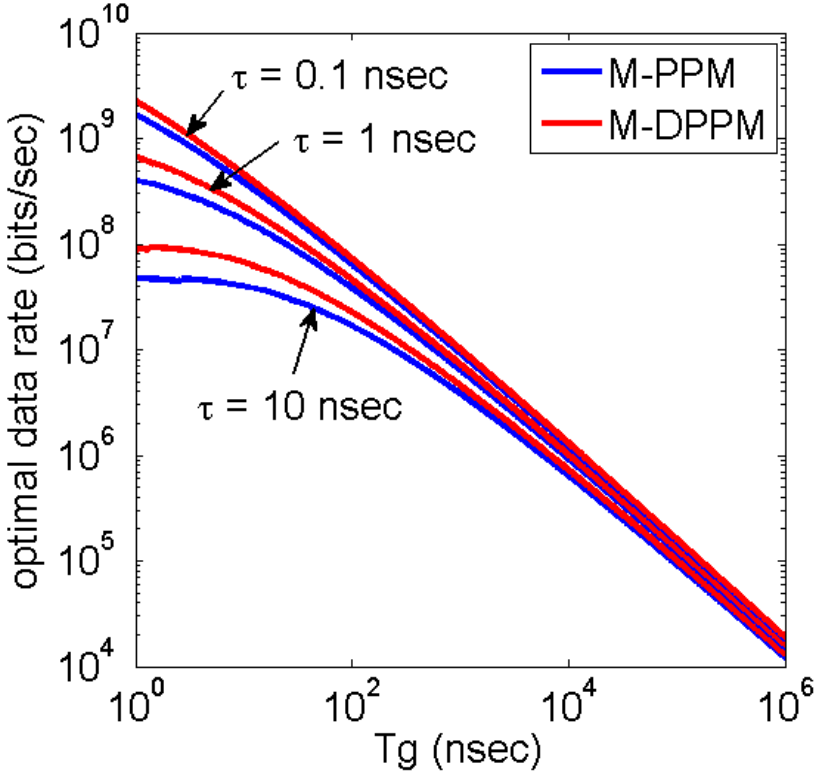
M-slot Differential Pulse Position Modulation

- Time is divided into slots of size τ.
- Guard time T_g placed after every pulse to ensure that laser is ready for next pulse.
- Pulse rising edge placed in one of *M* slots, transmitting one of *M* possible symbols.



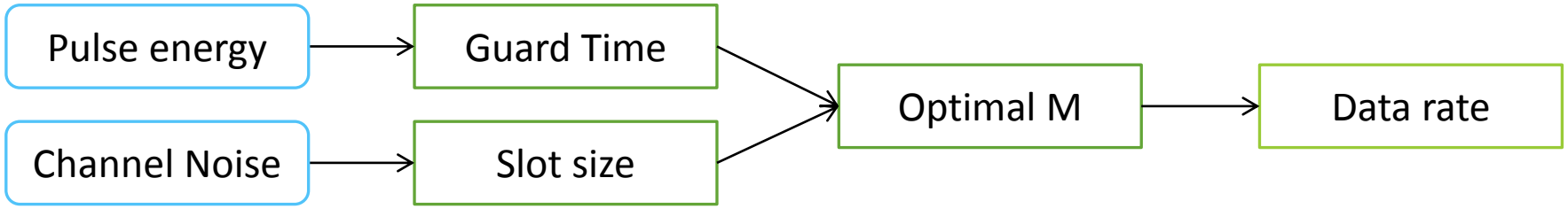
Optimal Number of Slots, *M*





An optimal *M* is chosen from required pulse energy and channel noise:

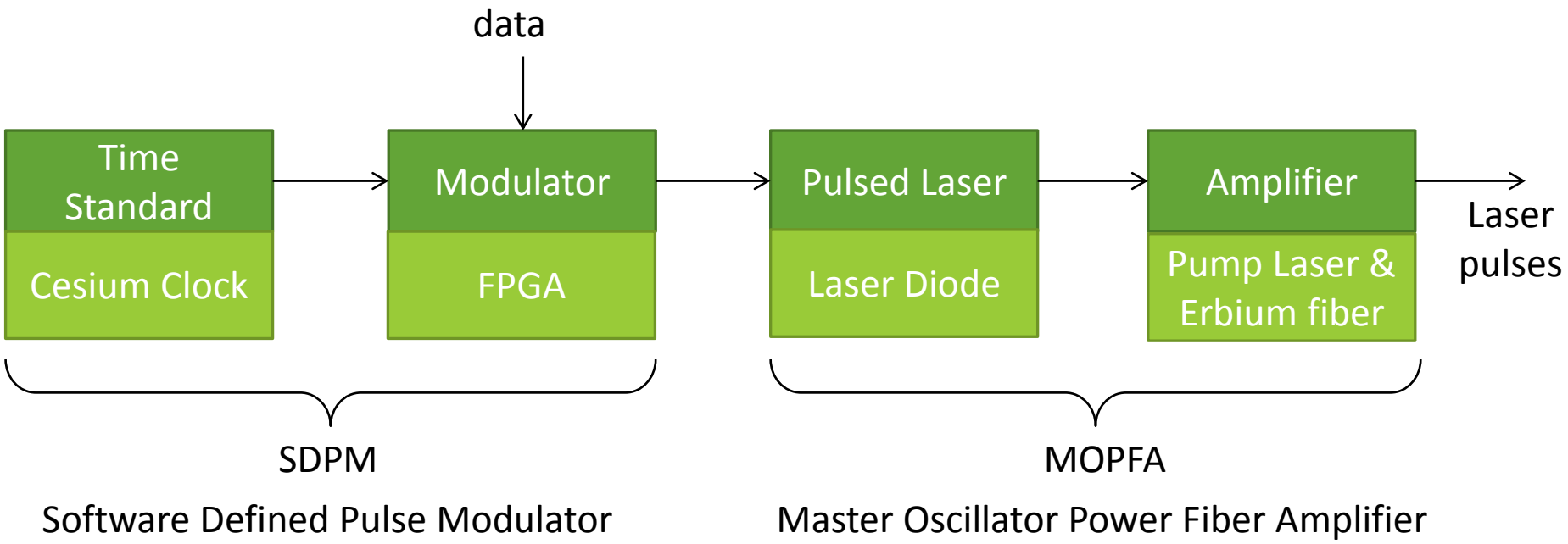
Requirements:



Structure

Two subsystems:

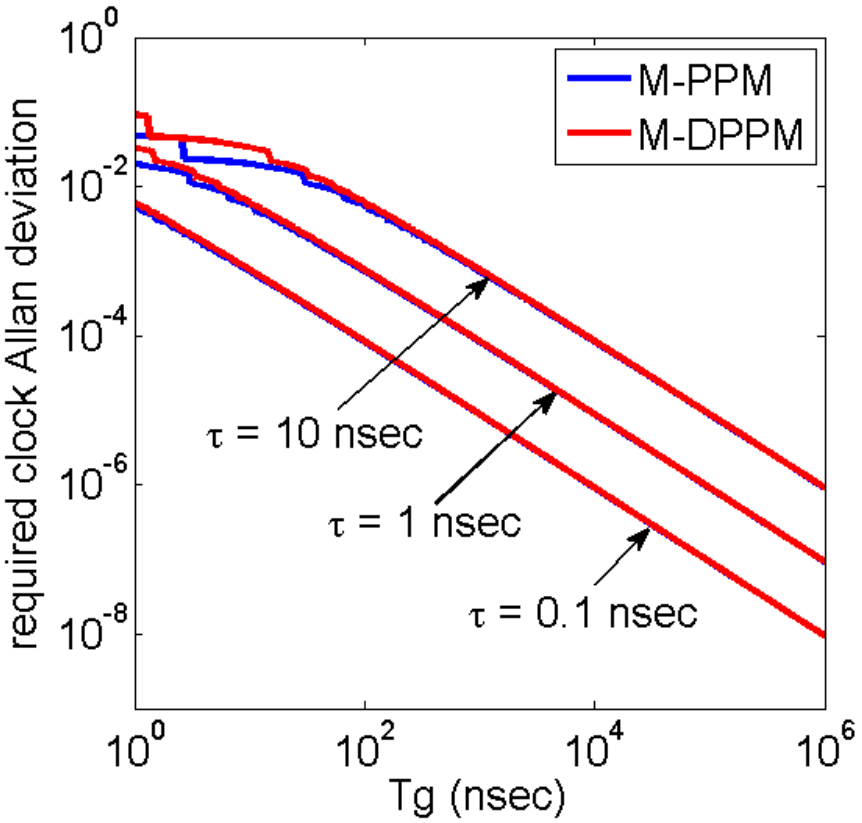
- Software Defined Pulse Modulator (SDPM)
  - Generate electric pulses according to the modulation scheme.
- Master Oscillator Power Fiber Amplifier (MOPFA)
  - Transform electric pulses into amplified light pulses.



Hardware: Time Standard

Characteristic	Chip Scale Atomic Clock (CSAC)
Standard	Cesium
Allan Deviation (time error)	3.3×10^{-12} @ 6000 sec (20 nsec)
Power	0.12 W
Mass	35 g
Size (LxWxH)	40.64 x 35.31 x 11.42 mm

CSAC in a CubeSat packaging



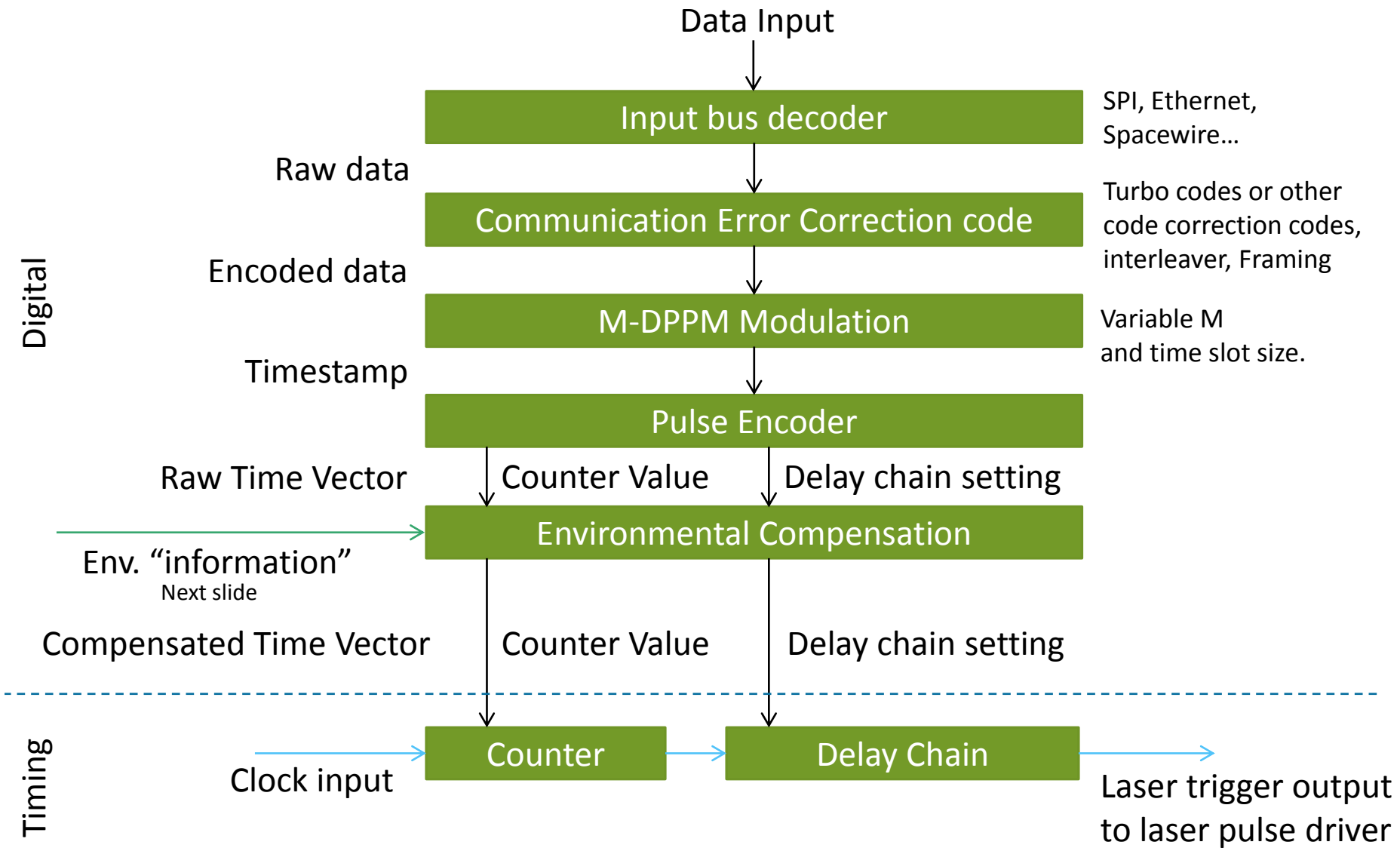
Hardware: FPGA

- Timing performance in FPGAs are very dependent of the platform:
  - FPGA selection must be done early.
  - Complete revalidation of timing section required if FPGA changes.
- Flash-based FPGA:
  - Reprogrammable: Allows part-to-part calibration.
  - Flash storage: No configuration upsets; No external programing.
  - Rad Tolerant version with same production process and structure.

SmartFusion®2

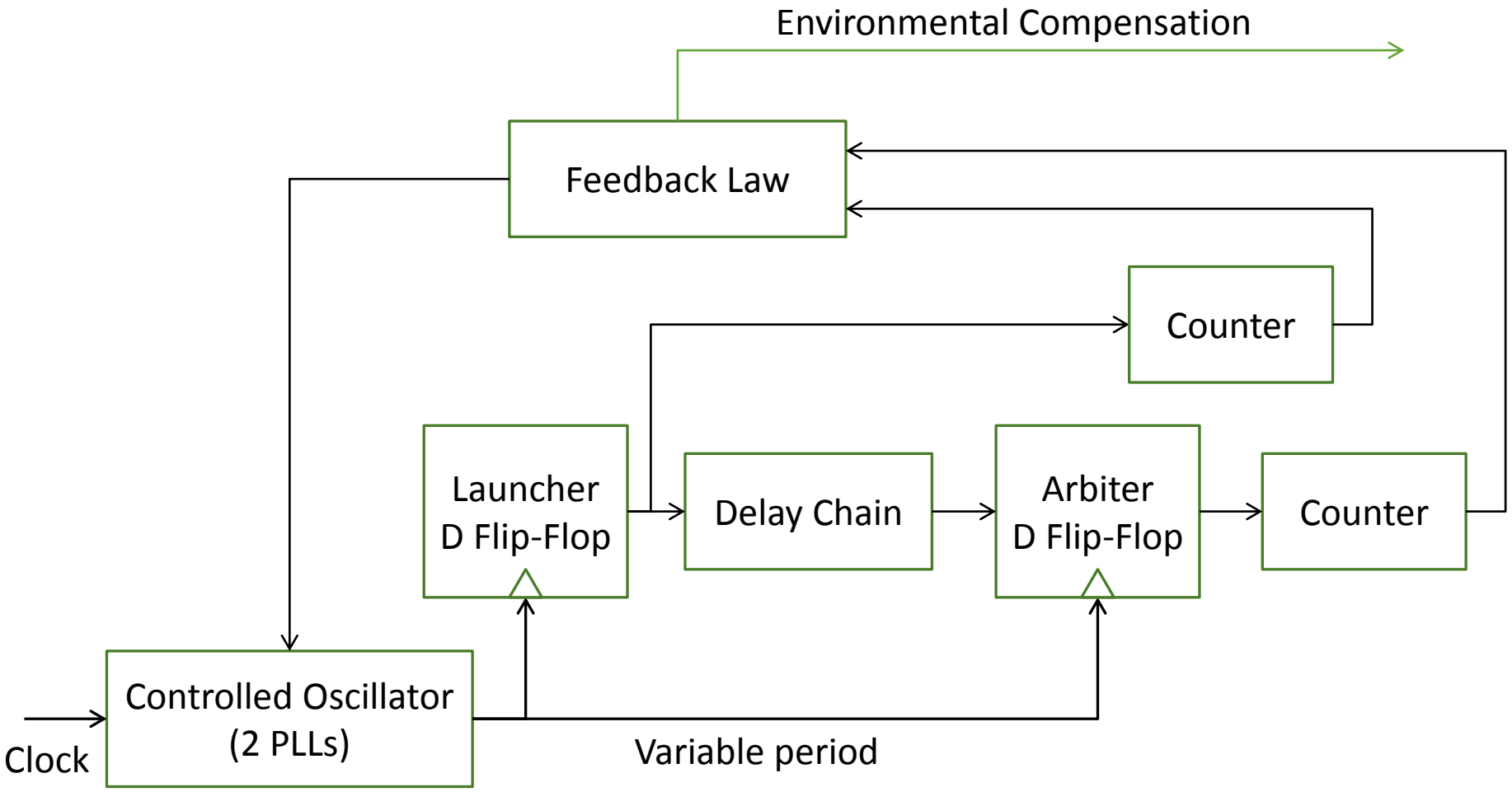
RTG4™

Modulator Data Flow

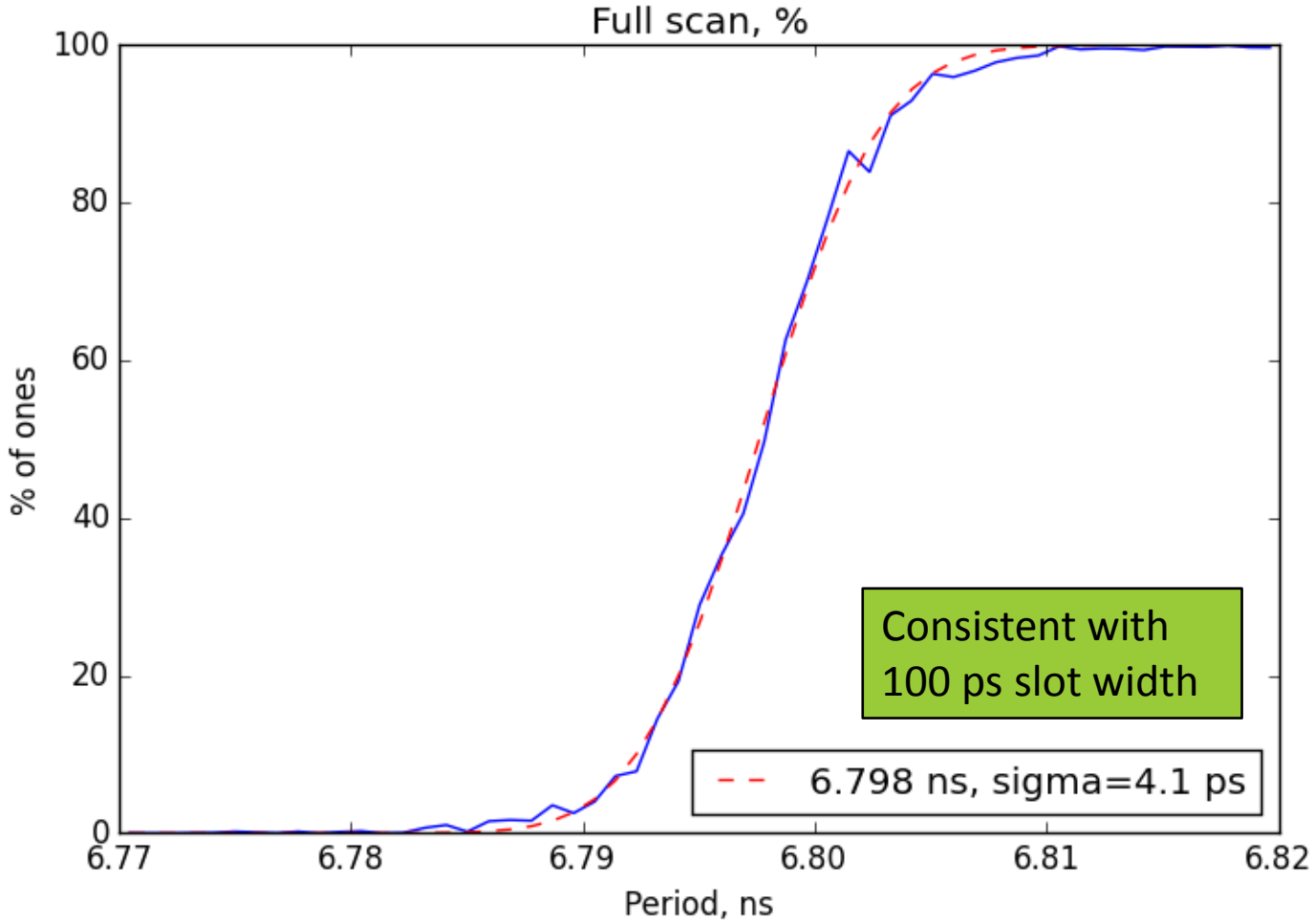


Environmental Compensation

- Temperature, voltage, radiation, aging $\rightarrow$ chain delay variations.
- Delay Locked Loop (DLL) measures delay variations.



Initial Results

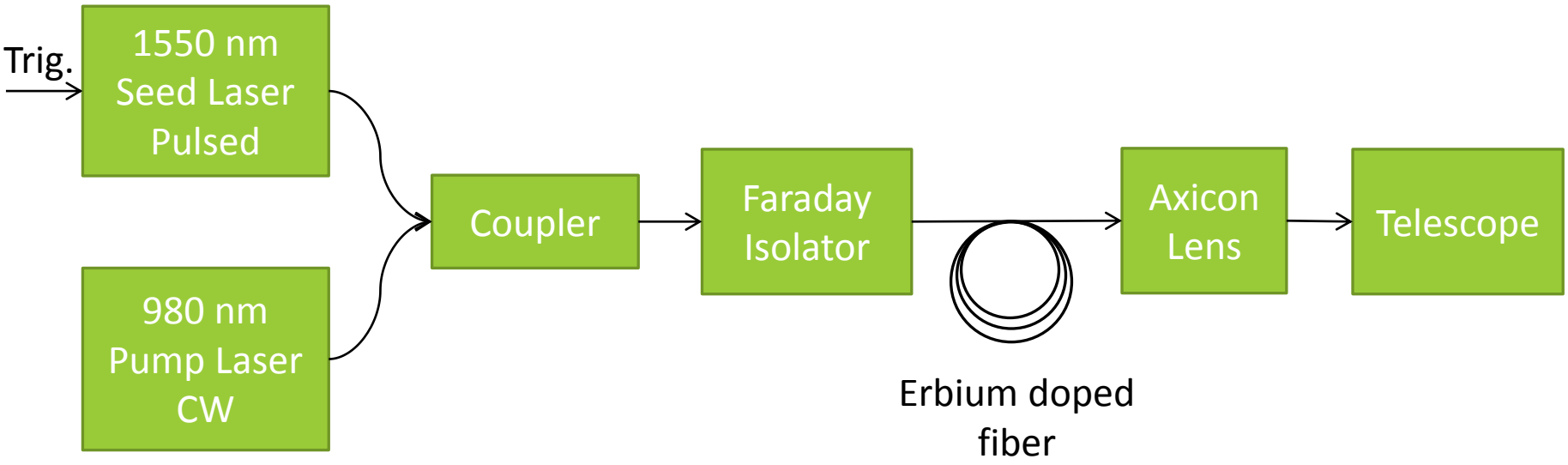


- Result from DLL circuit with 65280 samples per time (3×10^6 samples in 40 ms)
- Resolution of DLL oscillator: 1 ps typical, 2.3 ps worst case; Range: 4 to 24 ns.

Master Oscillator Power Fiber Amplifier

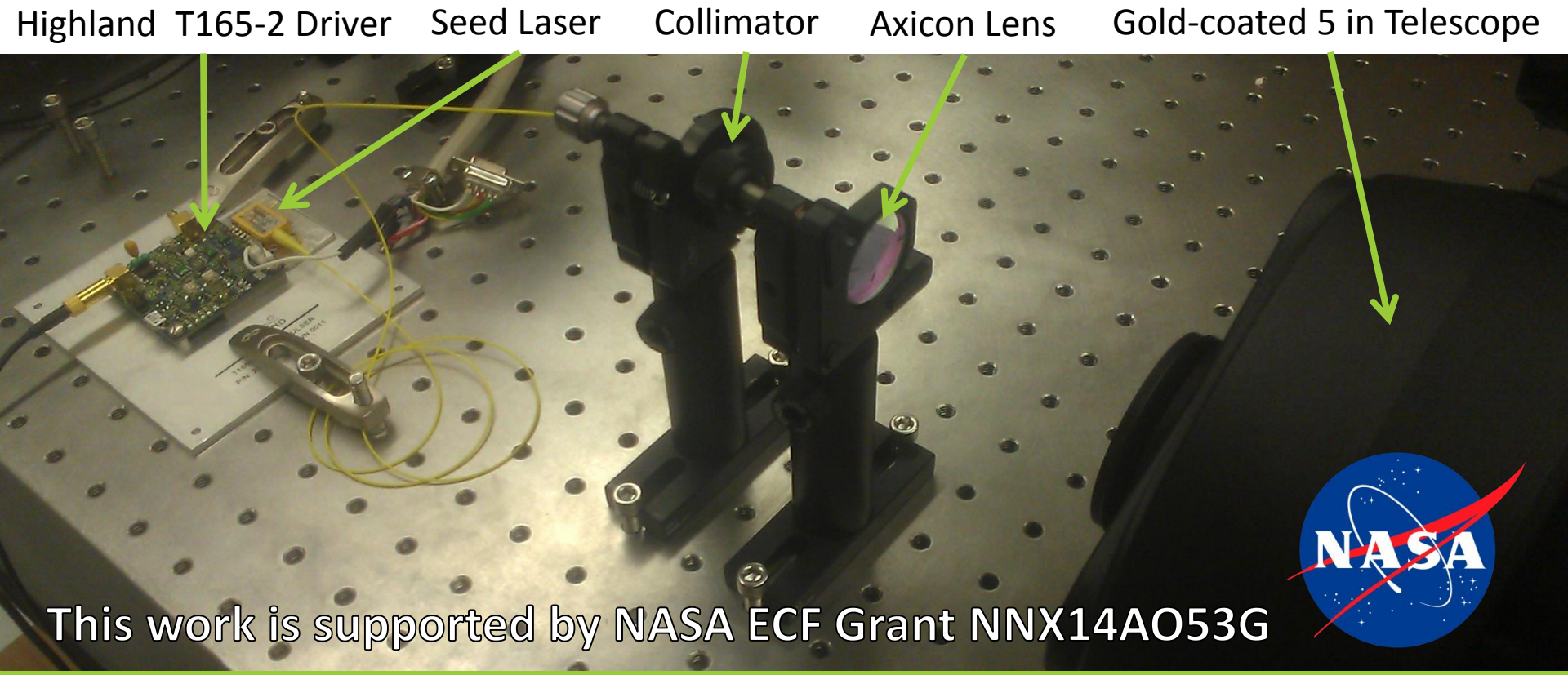
Erbium doped Fiber Laser

- High gain with low average power
- Maintains good beam quality
- Solid-state
- Compact



Conclusion

- Completed:
  - Automated modulator test bed
  - Delay chain design
  - Optical components selection and purchase
- Future work:
  - Low resolution data loopback with optics by August
  - Timing characterization in rad tolerant parts



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