

A Fault-Tolerant On-Board Computer For CubeSat Based-On Hybrid Architecture

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Friday, April 26, 2013 – Jérémy Delaporte

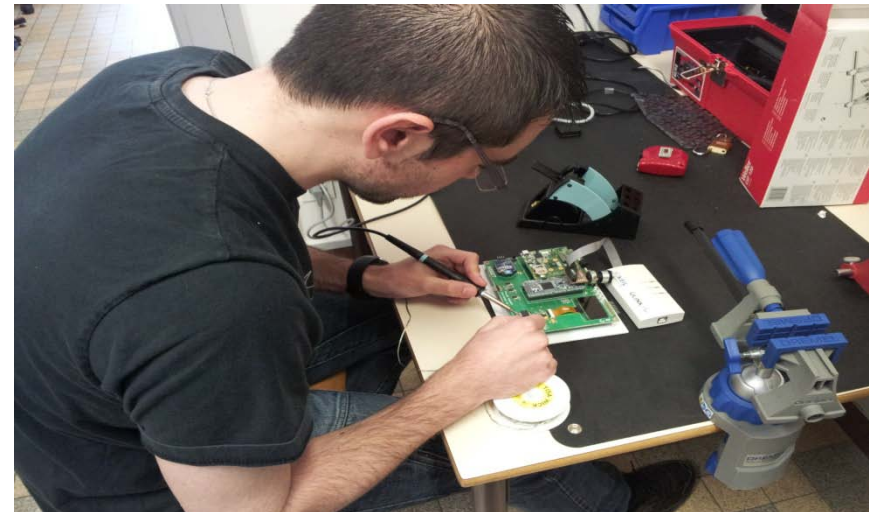
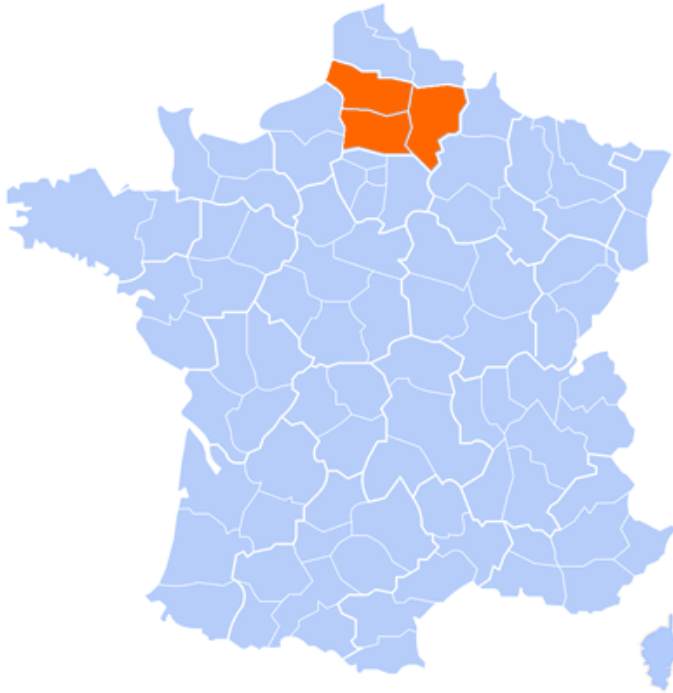




Outline

1. Institut Supérieur Des Sciences Et Techniques (INSSET - UPJV)
2. Space Environment – Effects On Electronic And Consequences
3. On-Board Computer For CubeSat
 1. Architecture And Mitigation Techniques
 2. Our Approach : Secure_ODB Project
4. Functional And Validation Tests
 1. Test Facilities
 2. Injection Faults Based-On JTAG Interface
 3. QB50 Project
5. Conclusion And Perspectives

Institut Supérieur Des Sciences Et Techniques (INSSET – UPJV)



Embedded Systems

Embedded Systems Department

Constraints & Architectures Design

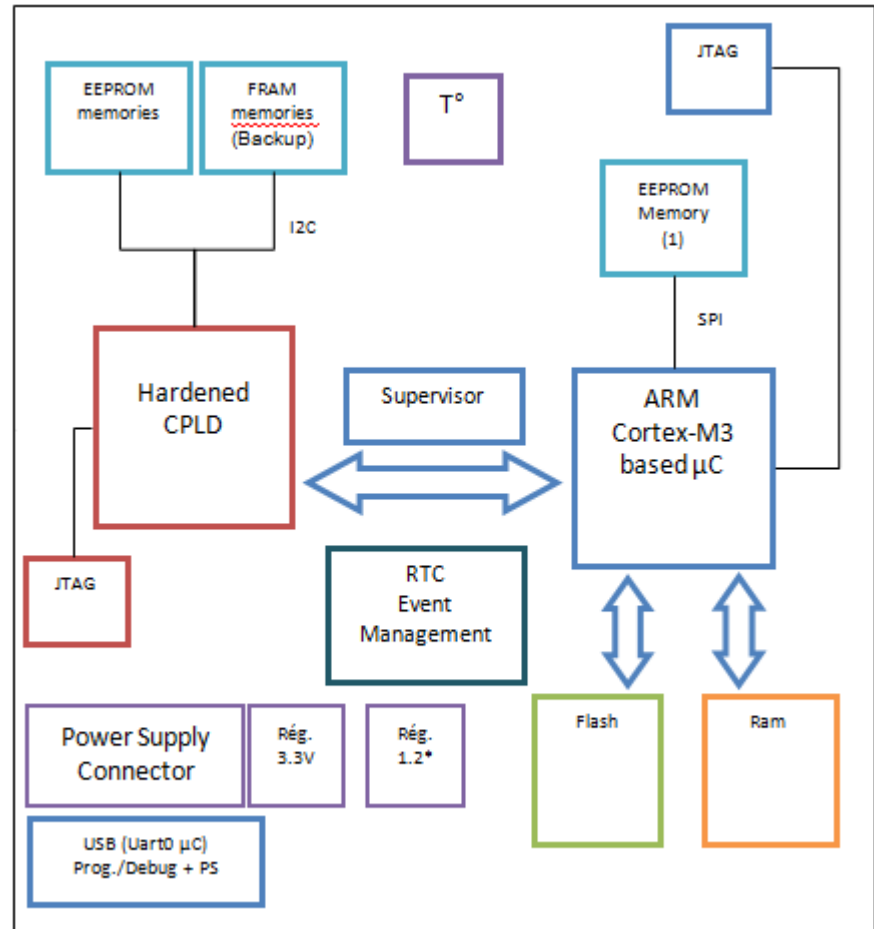
Embedded System



Constraints

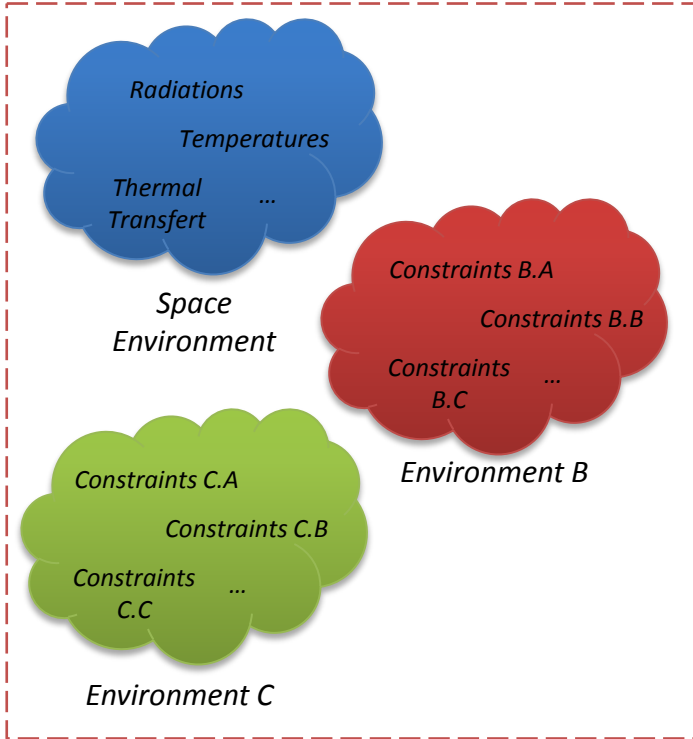
- Mass
- Cost
- Energy Consumption
- Performances
- Reliability Level
- Environmental
- Plug And Play (Modularity)
- Maintainability
- Memory
- ...

Architectures Design

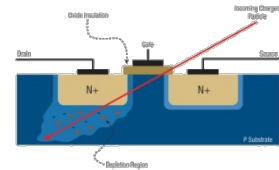




Embedded Systems And Reliability



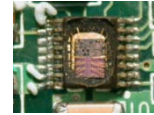
Constraints



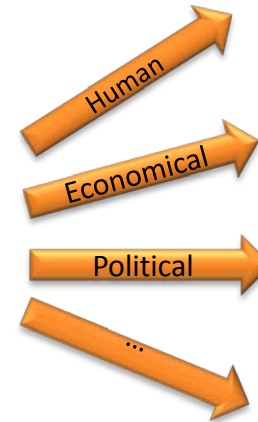
Effects

SEUs 0 -> 1
 1 -> 0

SEIs



Embedded Systems



...

Consequences

Space Environment Effects And Consequences On μ C

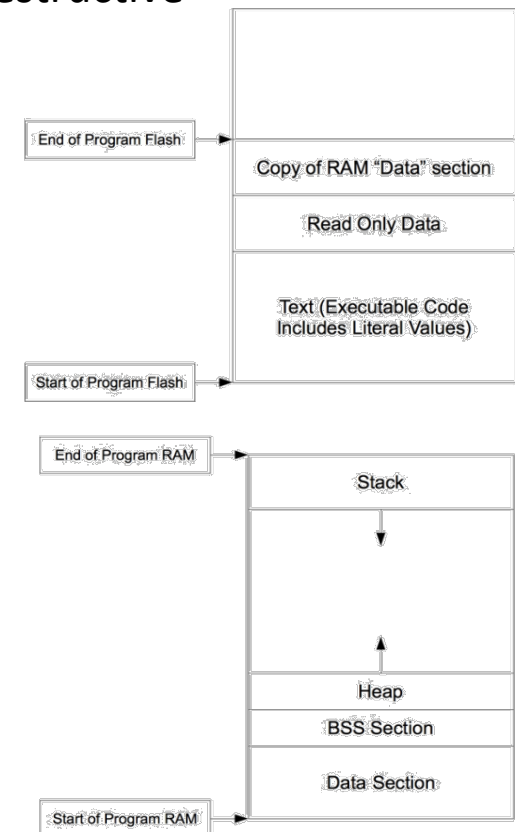
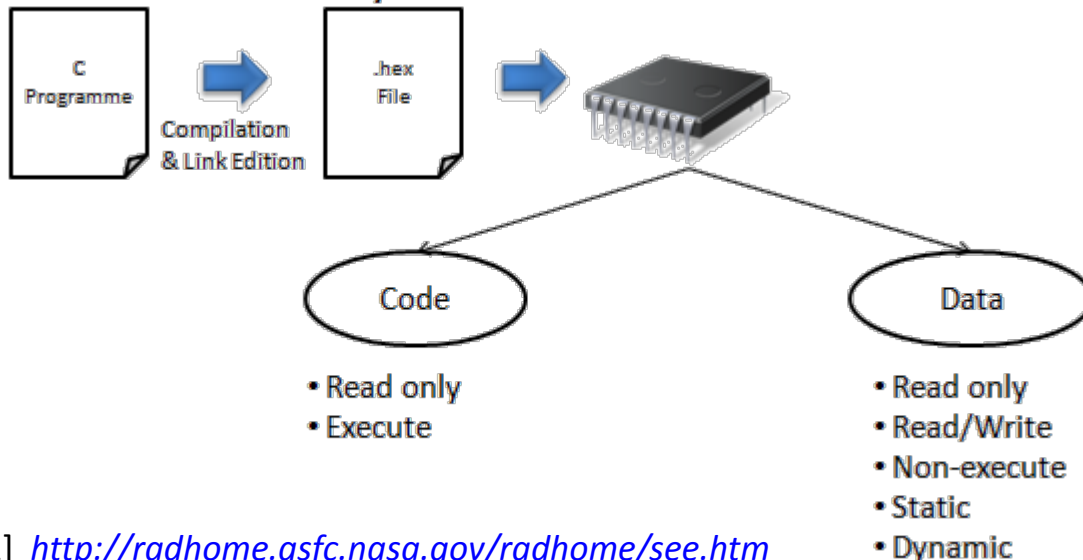
Effects

- Single Event Effects
 - **Single Event Upsets (SEUs) => Soft Errors And Non-destructive**
 - Single Event Latchups (SELs) => Hard Errors And “Destructive”
 - Single Event Burnout (SEBs) => Hard Errors And “Destructive”
 - ... See [1]

Transient pulses in logic
Bitflips in memory

Consequences

- Destruction of components
- Corruption of data



[1] <http://radhome.gsfc.nasa.gov/radhome/see.htm>

Mitigation techniques

“The goal of a fault-tolerant computer is to provide safety and liveness, **despite the possibility of faults.**” *Fault-Tolerant Architecture, Daniel Sorin – 2009*



Fig. 1 - Fault Tolerance Process

TABLE 2.1: The Three Types of Redundancy.

TYPE OF REDUNDANCY	BASIC IDEA	SINGLE EXAMPLE
Physical (spatial)	Add redundant hardware	Replicate a module and have the two replicas compare their results
Temporal	Perform redundant operations	Run a program twice on the same hardware and compare the results of the two executions
Information	Add redundant bits to a datum	Add a parity bit to a word in memory

Error Detection : REDUNDANCY

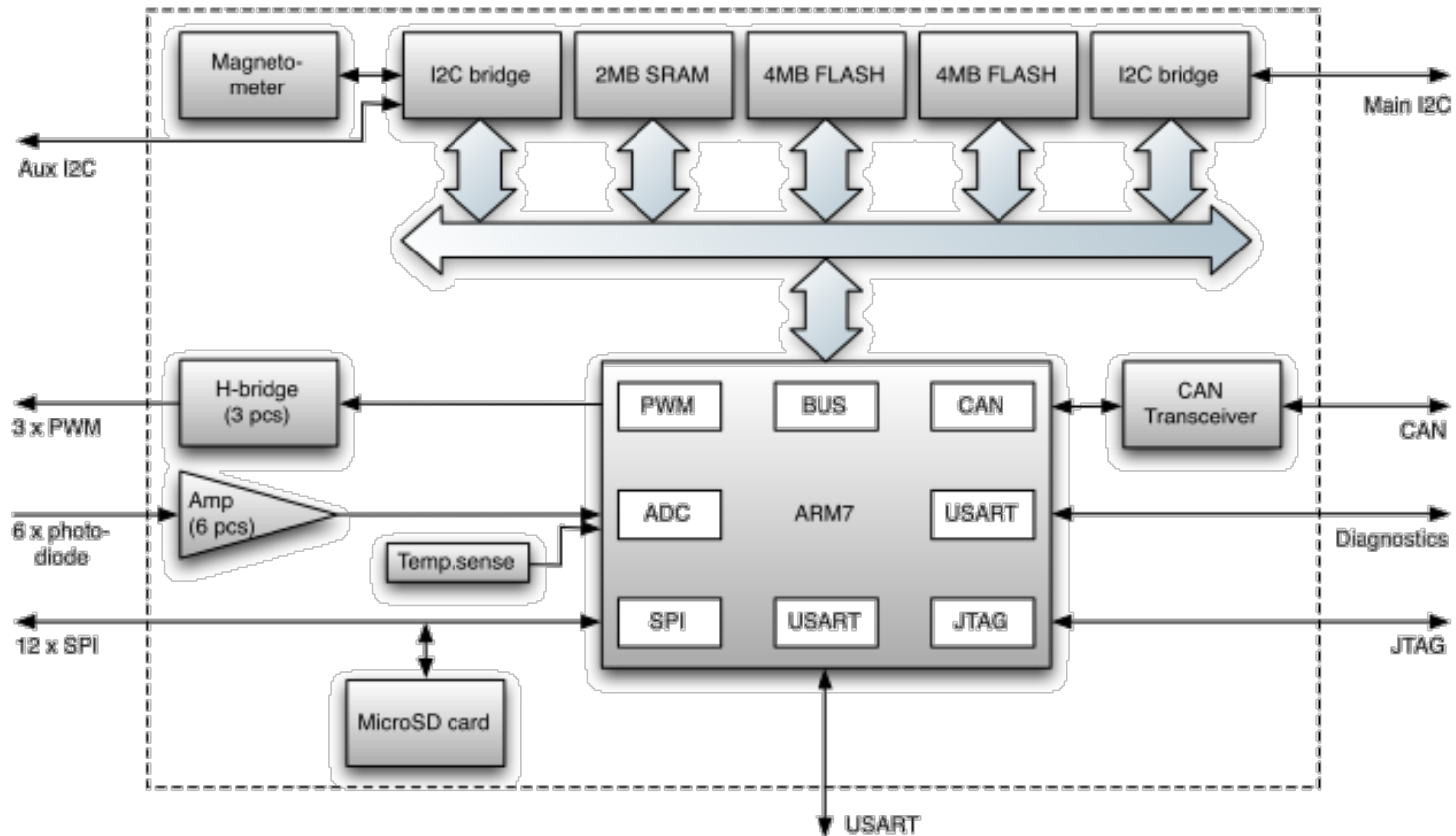


The use of detection techniques implies the system to be :

- More expensive
- Less performances
- Need more memory

On-Board Computer For CubeSat

General architecture



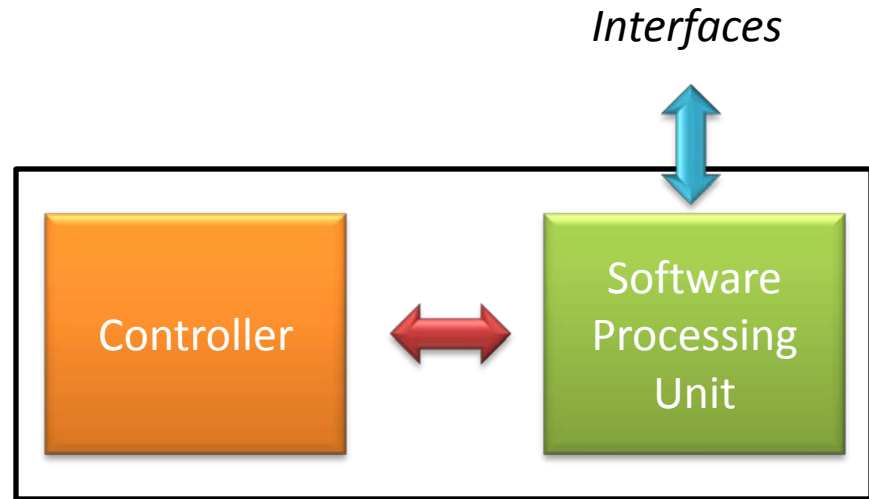
*NanoMind A712C Block Diagram
(GOMSPACE)*



On-Board Computer For CubeSat

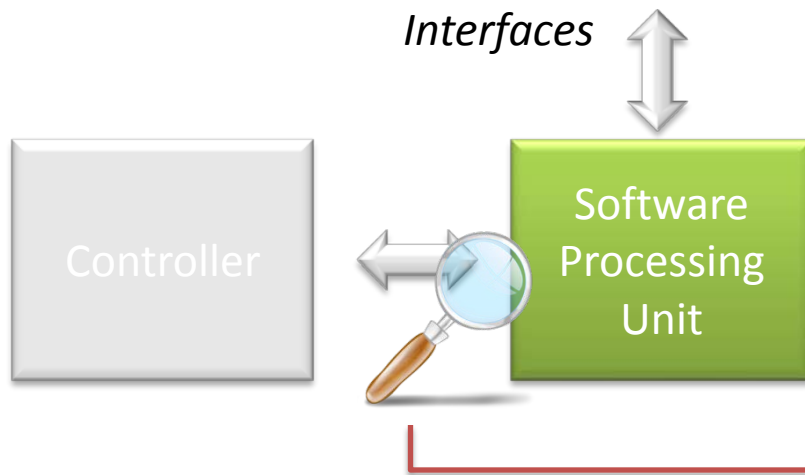
Our approach : Secure_ODB project (1/3)

1. Real-time overview of internal resources
 1. What is working or not
 2. Flash/RAM State
 3. Statistical information on errors
 4. ...
2. Estimation of threat based-on environment sensing : radiation & t° sensors (Need a calibration)
3. Dynamique reprogramming or reconfiguration of the Software Processing Unit

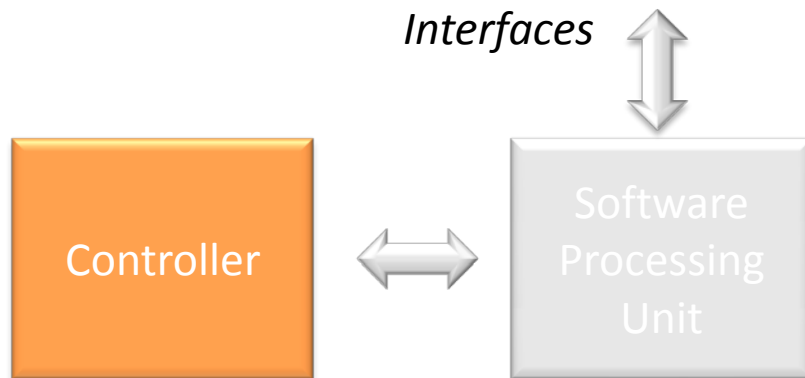
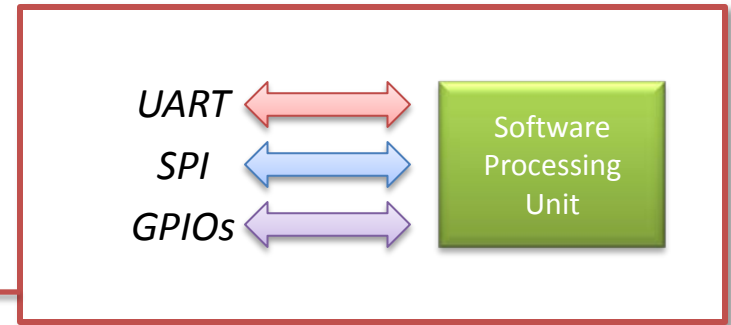


On-Board Computer For CubeSat

Our approach : Secure_ODB project (2/3)



- ARM Cortex-M3 Based μ C (NXP LPC1788)
- Boot loader in ROM Memory
- FreeRTOS



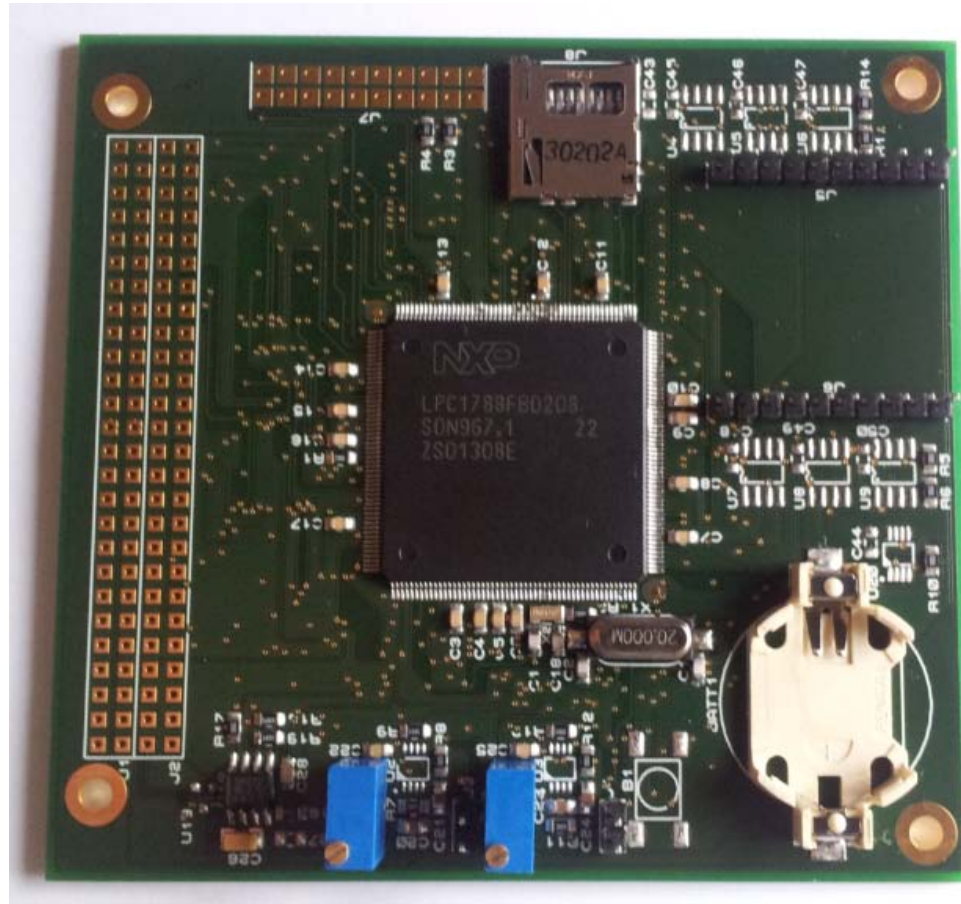
- Less performances than Software Processing Unit
- Reliable



Must be protected against energetic particles strikes (Radiation)

On-Board Computer For CubeSat

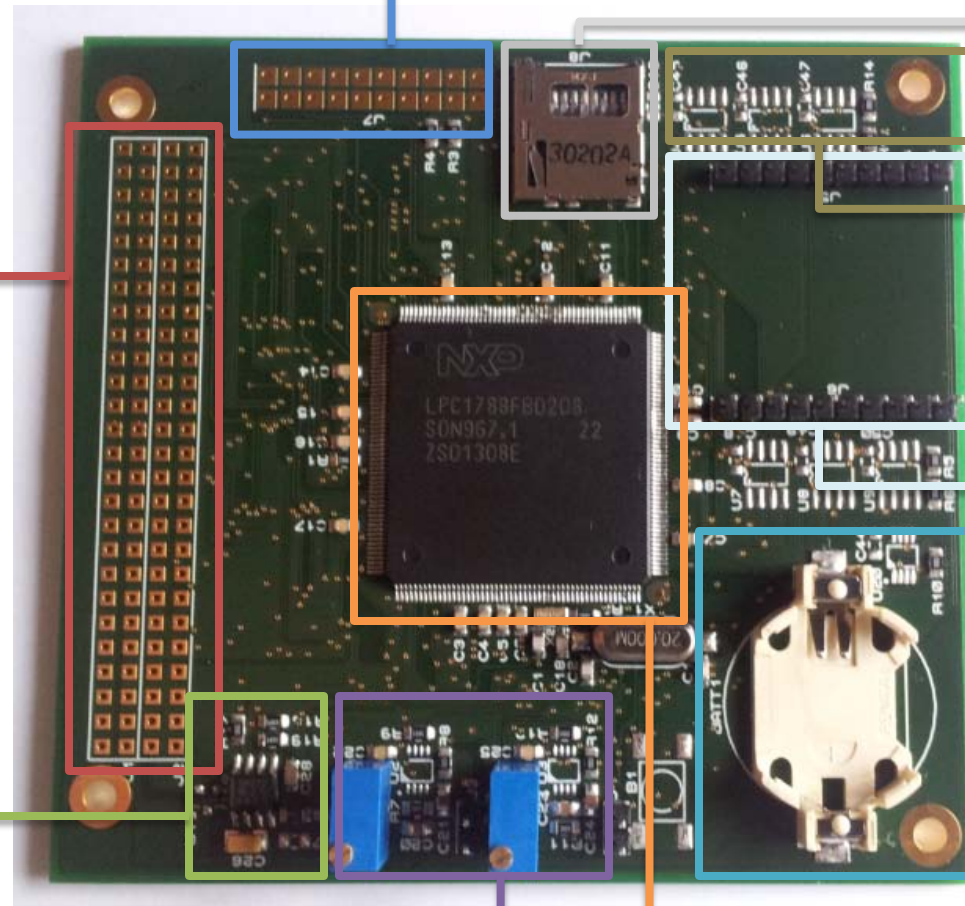
Our approach : Secure_ODB project (3/3)



Top view

On-Board Computer For CubeSat

Our approach : Secure_ODB project (3/3)



JTAG

μSD Socket

CubeSat Kit Bus Connector

EEPROM/FRAM* Memories

Controller Interface

CAN Transceiver

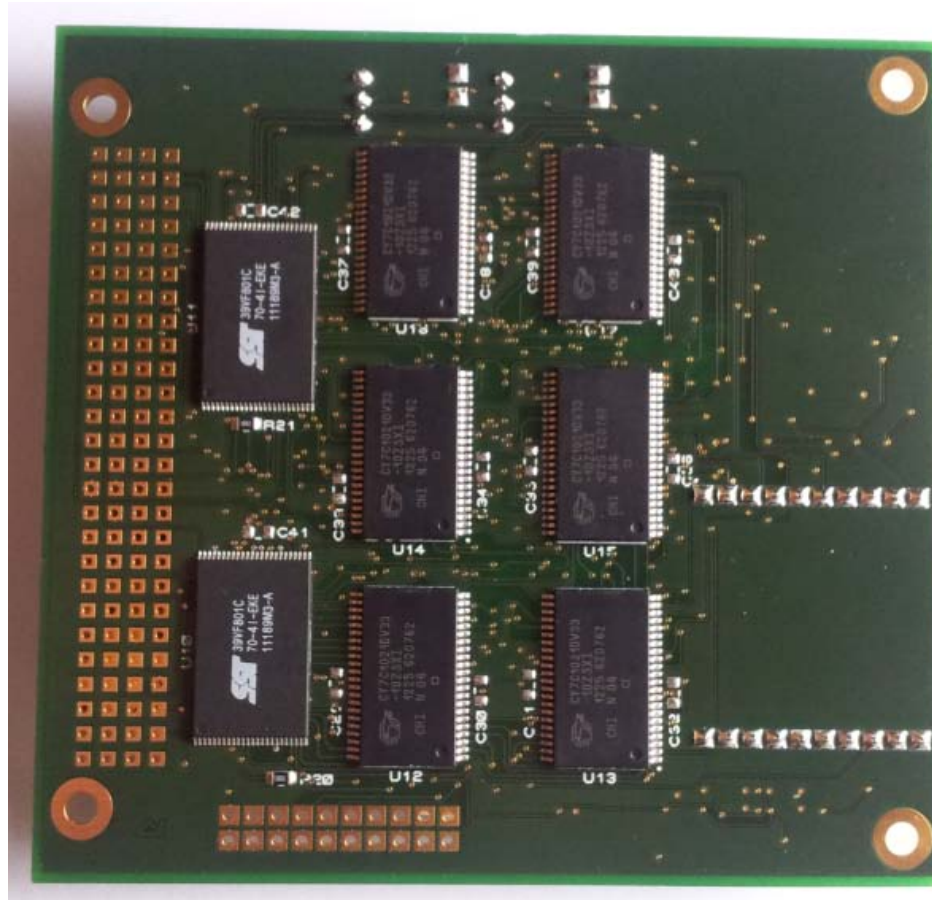
RTC Battery

Controller & μC Supervisors

Cortex-M3 Based μC

On-Board Computer For CubeSat

Our approach : Secure_ODB project (3/3)

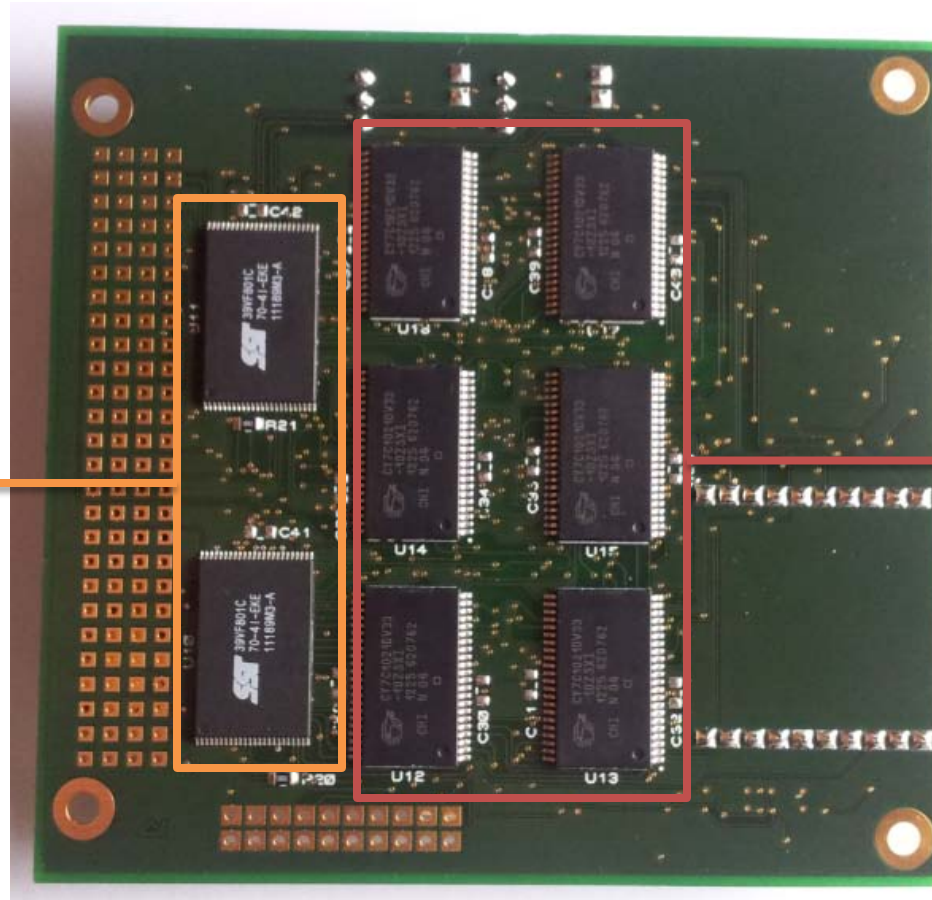


Bottom view

On-Board Computer For CubeSat

Our approach : Secure_ODB project (3/3)

External Flash
Memories

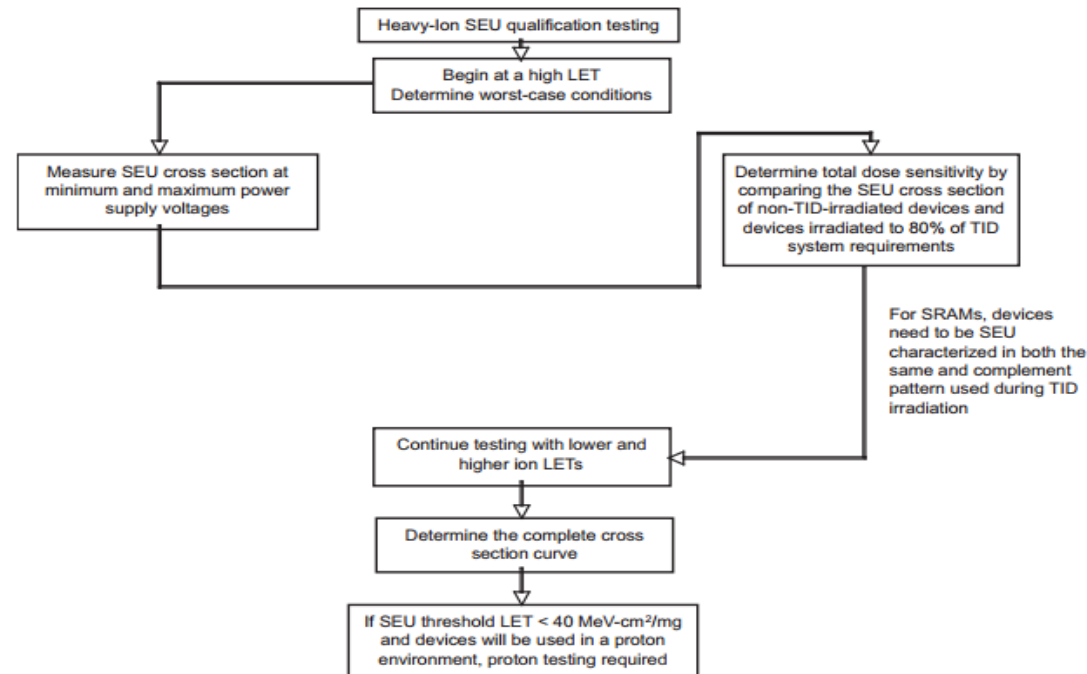


External RAM
Memories

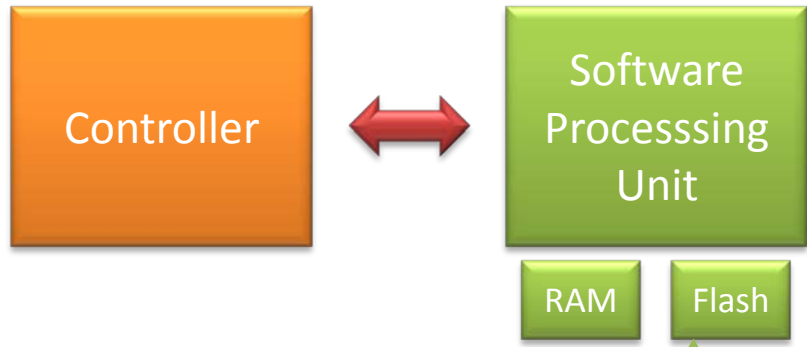
Functional And Validation Tests

Test Facilities

- Brookhaven National Laboratory SEUTF (heavy ion)
- Lawrence Berkeley Labs 88" Cyclotron (heavy ion)
- Texas A & M University Cyclotron (heavy ion)
- Paul Scherrer Institute (heavy ion)
- University of California at Davis Crocker Nuclear Lab (proton)
- Indiana University Cyclotron (proton)
- ...



Functional Tests And Validation



JTAG-Based Injection Fault System

Configuration

Adresse du début de la RAM: 0x10000000
Longueur de la RAM: 0x7FF

Méthode: Dynamique
Scénario: Explorer

Mode manuel: Adresse: Nombre d'erreurs: 1
BR: 0 Durée: 10 s

Log

Copy On Chip Debugger 0.3.0 (2011-12-03-08:57)
Licensed under GPL v2
For bug reports, mail: http://spencer.berlios.de/bug-tracker/bug.html
info: only one hardware option allowed! JTAG
adapter_name: oklay-300
freq: 4000000
10 kHz



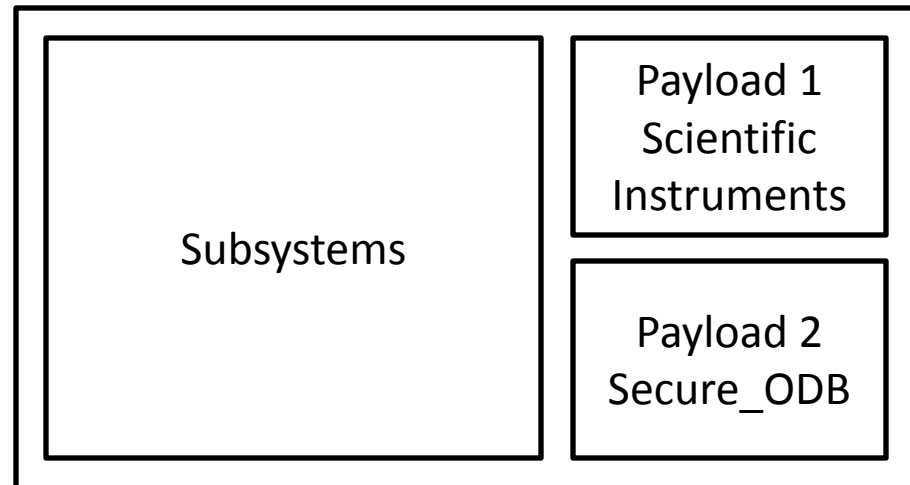
Functional Tests And Validation

QB50 project

“QB50 has the scientific objective to study in situ the temporal and spatial variations of a number of key constituents and parameters in the lower thermosphere (90-320 km) with a network of about 40 double CubeSats, separated by a few hundred kilometres and carrying identical sensors.”



- Launch scheduled in 2015





Conclusion And Perspectives

- On-Board Computer (Prototype 1) has just been done
 - Functional tests will be perform next weeks
 - Validation tests (QB50 or Facility tests)
- Definitive choice of the controller (doctor) : CPLD, μ C 8-bits, other ?
- Contact Marquette University => Similar hardware architecture
- Questions ?