LANL CubeSat Reconfigurable Computer (CRC)

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Los Alamos National Laboratory (LANL)

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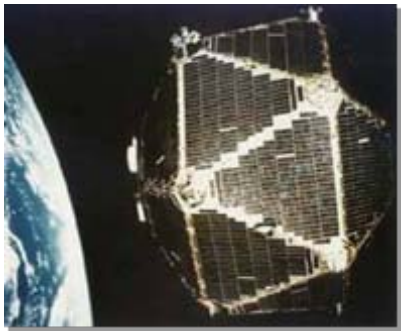
LANL history in space

Operational Sensors

Vela W-Sensor



GPS IIA/IIR W-Sensor

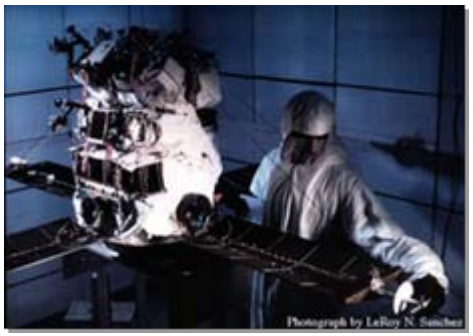
GPS IIF V-Sensor

CubeSat ?

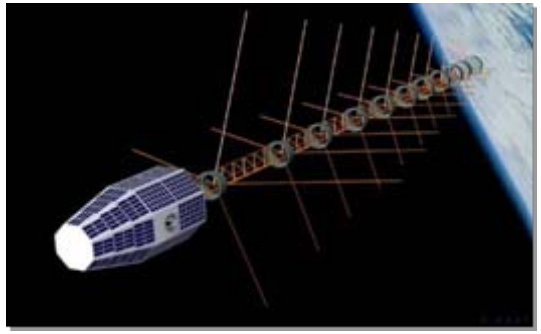
http://en.wikipedia.org/wiki/File:CP4_in_flight.jpg

R&D Sensors

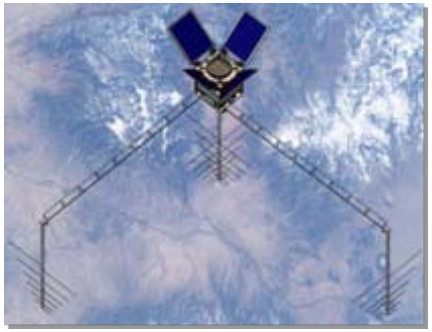
ALEXIS/Blackbeard



FORTE



Cibola Flight Experiment



Cibola Flight Experiment (CFE)

- **Project Objectives**
  - Technology Demonstration: responsive, flexible multi-mission RF payload with continuous data processing
    - Reconfigurable Computing (RCC) technology for super-computer processing speeds at sensor
    - Adaptability: Re-configurable post-launch
  - Smart and adaptive computing at sensor for enhanced sensitivity and reduced data downlink
- **Technical Approach**
  - On-board data processor using COTS parts
    - Networks of Xilinx Field Programmable Gate Arrays (FPGA)
    - FPGA's allow post-launch reconfiguration to meet new and changing program requirements
    - New digital signal processing applications developed on the ground are uploaded to the payload for execution
    - Tailor processing application to each theater of interest
      - Algorithms swap time <1 min
- **Payload Description**
  - 4-Channel Software Radio
    - Tunable 100-500 MHz with 20 MHz bandwidth
  - Dual 12-bit ADC @ 100 Msps

Adaptive technology on CubeSats

Prior experience

- Reconfigurable FPGAs: 100 – 1000x the performance of a microprocessor
- LANL has CFE & other mission experience
- LANL is a leader in SRAM FPGA SEU testing and mitigation
- Miniaturization
- Integration into a SOC & single or few PCBs

Reconfigurable functionality for each satellite

- *HW reuse* enhances reliability and decreases cost, increases the code base and accelerated development time.

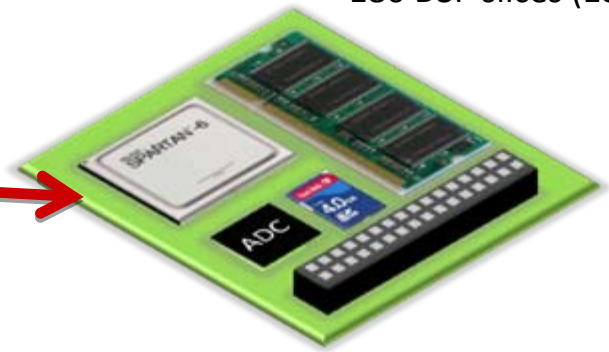
Using CubeSats

- High performance, low power computing in a small form factor
- Data-intensive signal processing is an ideal application
- Upgrade or add functionality after launch
- Simplifies the hardware design for CubeSat constellations

Miniaturization

	Cibola Flight Experiment	CubeSat Reconfigurable Computer
Size	16” x 8” x 12”	4” x 4” x 1”
Weight	20 kg	100 g
Power	100 W	10 W
Logic Density	219K registers	185K registers*
Speed	50 MHz	100MHz
On-chip memory	1Mb	5Mb
System memory	.86 GB	.5 GB
Sample Rate	100 Msps	250 Msps
# bits	12	12
# Channels	2	2

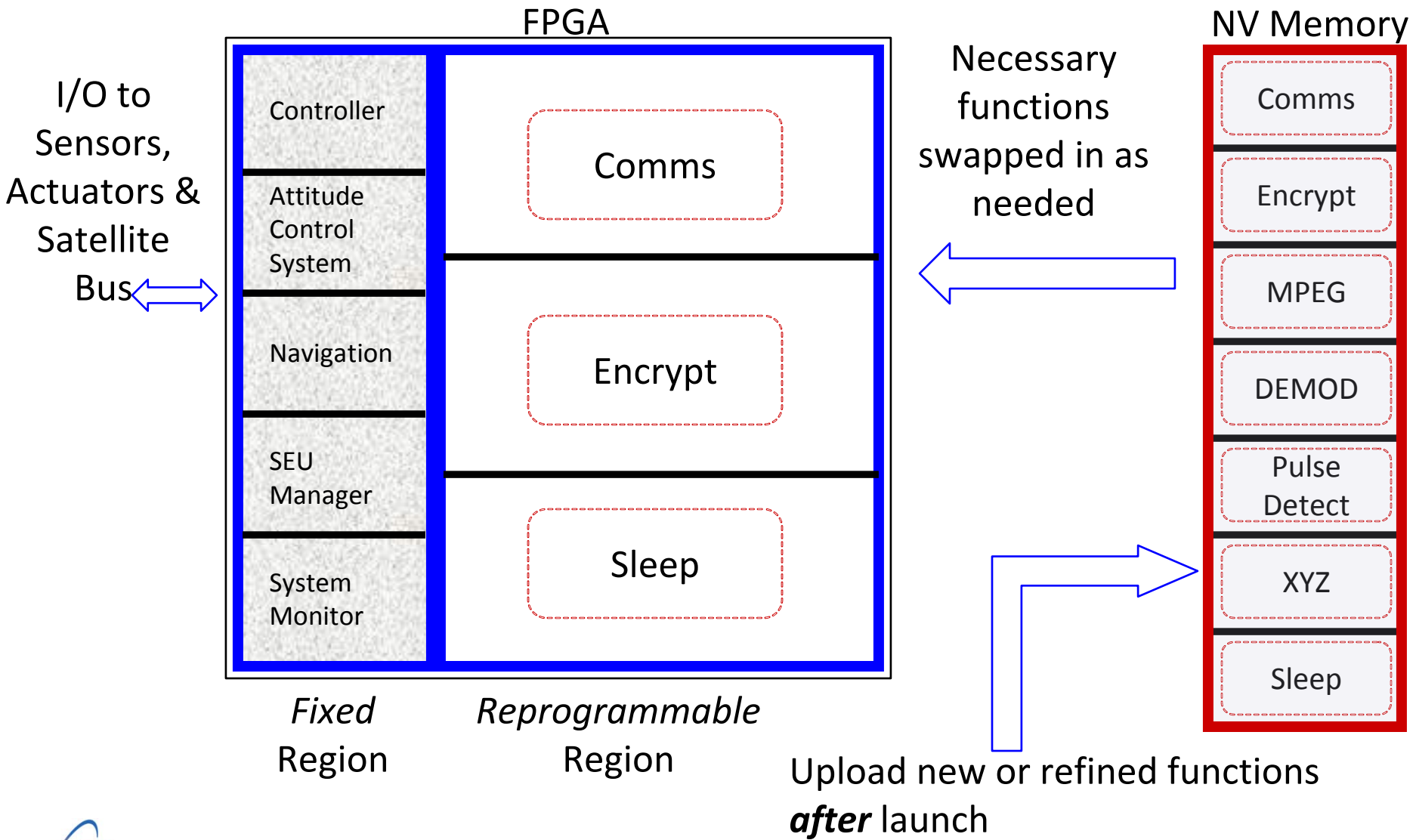
*+180 DSP slices (18*18 MAC)



CRC board design

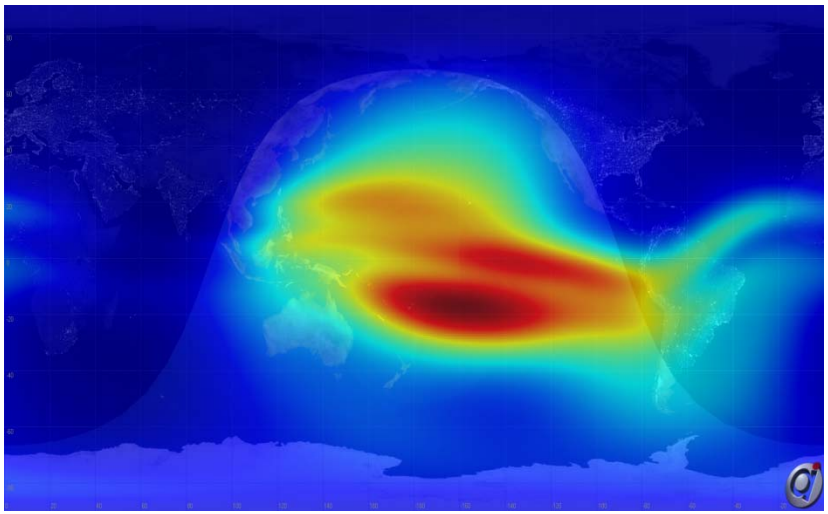
- **Miniaturization of CFE Satellite Payload**
  - More capable than all CFE instrument FPGAs
  - More capable than the CFE follow-on instrument
  - Reduced lifecycle allows more relevant technology to orbit
- **Xilinx Spartan-6**
  - More power efficient than Xilinx Virtex-6
  - Very little performance loss for smaller chips

Partial Reconfiguration:
"Software Defined Satellite" => Extreme Integration



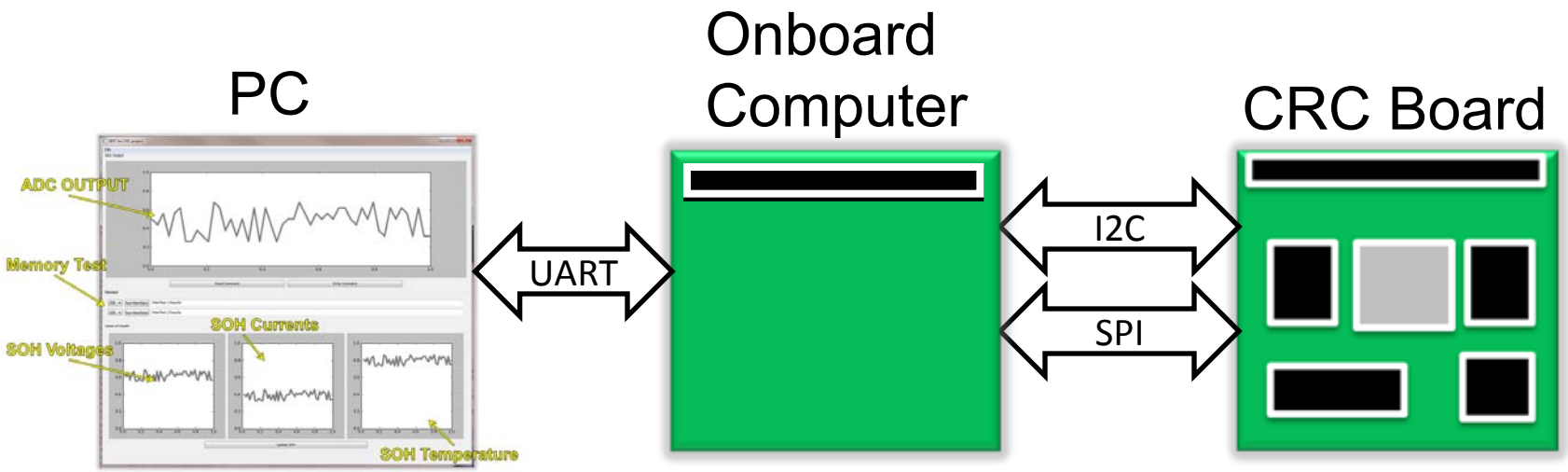
Science Mission

- **Measure Total Electron Content (TEC) in Ionosphere**
  - Wide band RF pulse detection
  - TEC tomography using lightning strikes and generated signals
  - Test signals generated from the laboratory and transmitted to orbiting satellites
  - Joint space and ground observations are combined for generating measurements



http://en.wikipedia.org/wiki/File:IRI_TotalElectronContent.png

Built-in Self-Test (BIST) development setup



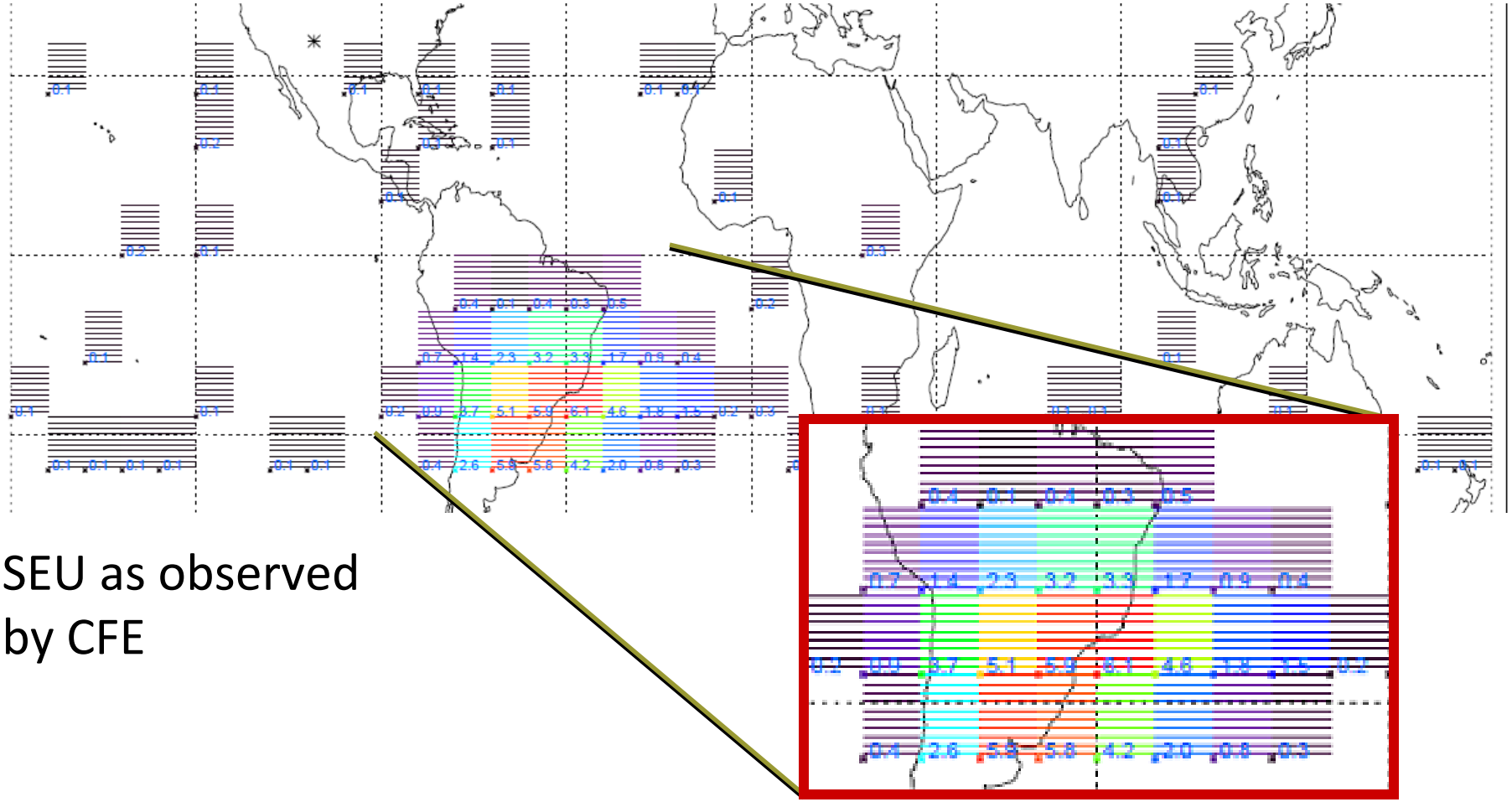
Testing

- BIST can be ran without a PC, directly from the onboard computer for on orbit testing
- BIST checks CRC board for:
  - Opens
  - Shorts
  - Signal integrity
  - Memory interfaces
  - ADC interfaces
  - ADC performance

Current Status

- **Hardware**
  - Received CRC board from manufacturing 7/26/2010
  - Powered on and basic functionality verified
  - Further testing to be completed before full functionality is verified
- **Software**
  - GUI for BIST to verify CRC boards nearing completion
  - First FPGA configuration designed to read and report ADC readings nearing completion

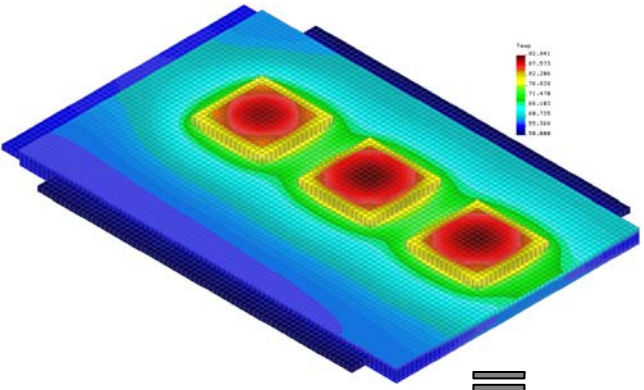
Challenge 1: Configuration SEUs / Device Day/ Cell



SEU as observed by CFE

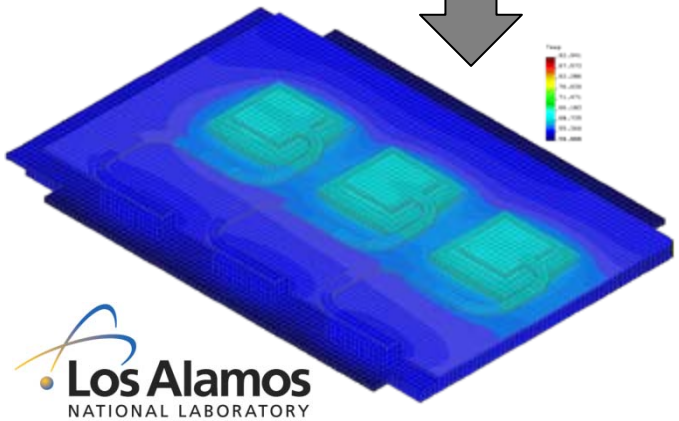
Challenge 2: Power Consumption (Thermal) = f(algorithm)

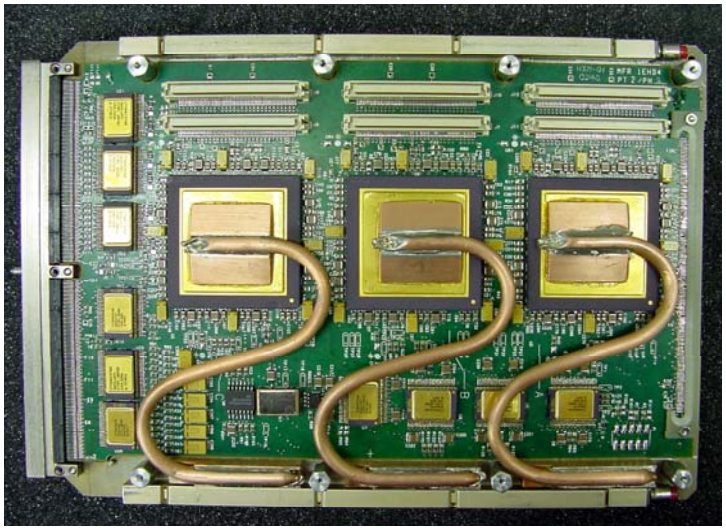
- **Each RCC board power usage ≈5 - 28W**
- **Each FPGA has >500 pins which are susceptible to thermal stresses**
  - Maximize lifetime
    - Heat pipes limit max temperatures
    - Column Grid Array package more reliable
    - Matched CTE of thermount PCB to Ceramic Pkg
    - AlBeMet core has superior thermal transfer



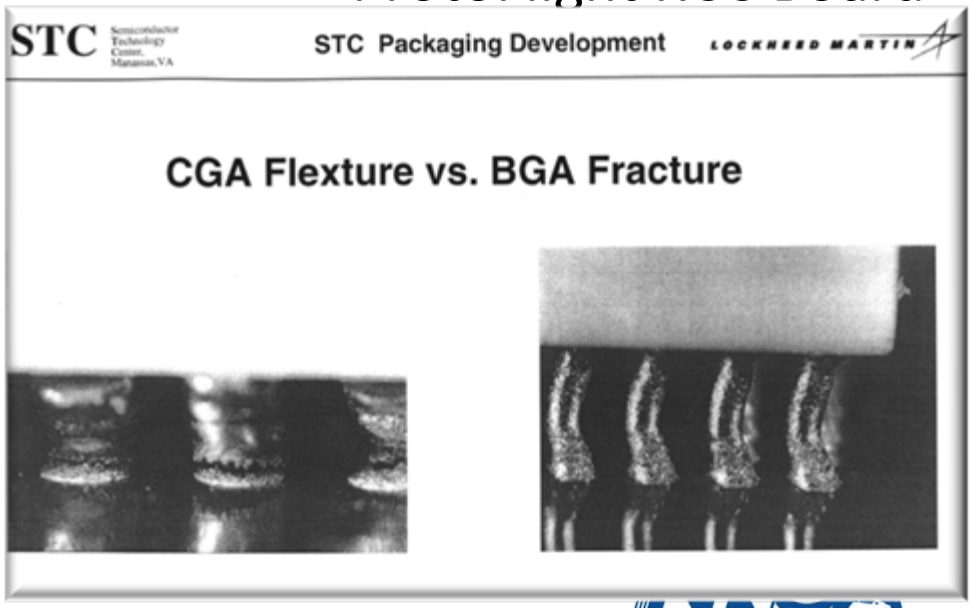
Without heat pipes:
Δt=50 deg C

With heat pipes:
Δt=17 deg C





ProtoFlight RCC Board



Future Work

- **Constellations**
  - Numerous inexpensive satellites replace larger expensive satellites
  - Paradigm shift allows new functions to be performed
    - Spatial separation
    - Unit replacement
  - True global and persistent observation

Conclusion

- **Reconfigurable Processing**
  - Unparalleled performance
  - Extreme integration
  - Very flexible for various satellite missions and configurations
  - Upgradeable after launch
  - Serve multiple users with a single platform
- **CubeSats may allow synchronization between technology nodes and launch schedules**
  - More appropriate technology insertion schedules
- **Challenges:**
  - Need a more systematic thermal management design for high power density applications with wild swings in power consumption
  - Keep radiation tolerance and SEU management in mind
  - Small is not necessarily simple; complexity is still an issue