LANL CubeSat Reconfigurable Computer (CRC)
LANL history in space

Operational Sensors

Vela W-Sensor

GPS IIA/IIR W-Sensor

GPS IIF V-Sensor

R&D Sensors

ALEXIS/Blackbeard

FORTE

Cibola Flight Experiment

CubeSat ?

Cibola Flight Experiment (CFE)

- **Project Objectives**
  - Technology Demonstration: responsive, flexible multi-mission RF payload with continuous data processing
    - Reconfigurable Computing (RCC) technology for super-computer processing speeds at sensor
    - Adaptability: Re-configurable post-launch
    - Smart and adaptive computing at sensor for enhanced sensitivity and reduced data downlink

- **Technical Approach**
  - On-board data processor using COTS parts
    - Networks of Xilinx Field Programmable Gate Arrays (FPGA)
    - FPGA’s allow post-launch reconfiguration to meet new and changing program requirements
    - New digital signal processing applications developed on the ground are uploaded to the payload for execution
    - Tailor processing application to each theater of interest
      - Algorithms swap time <1 min

- **Payload Description**
  - 4-Channel Software Radio
    - Tunable 100-500 MHz with 20 MHz bandwidth
  - Dual 12-bit ADC @ 100 Mspi
Adaptive technology on CubeSats

- Prior experience
  - Reconfigurable FPGAs: 100 – 1000x the performance of a microprocessor
  - LANL has CFE & other mission experience
  - LANL is a leader in SRAM FPGA SEU testing and mitigation
  - Miniaturization
  - Integration into a SOC & single or few PCBs

- Reconfigurable functionality for each satellite
  - *HW reuse* enhances reliability and decreases cost, increases the code base and accelerated development time.

- Using CubeSats
  - High performance, low power computing in a small form factor
  - Data-intensive signal processing is an ideal application
  - Upgrade or add functionality after launch
  - Simplifies the hardware design for CubeSat constellations
# Miniaturization

<table>
<thead>
<tr>
<th></th>
<th>Cibola Flight Experiment</th>
<th>CubeSat Reconfigurable Computer</th>
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<tbody>
<tr>
<td><strong>Size</strong></td>
<td>16” x 8” x 12”</td>
<td>4” x 4” x 1”</td>
</tr>
<tr>
<td><strong>Weight</strong></td>
<td>20 kg</td>
<td>100 g</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>100 W</td>
<td>10 W</td>
</tr>
<tr>
<td><strong>Logic Density</strong></td>
<td>219K registers</td>
<td>185K registers*</td>
</tr>
<tr>
<td><strong>Speed</strong></td>
<td>50 MHz</td>
<td>100MHz</td>
</tr>
<tr>
<td><strong>On-chip memory</strong></td>
<td>1Mb</td>
<td>5Mb</td>
</tr>
<tr>
<td><strong>System memory</strong></td>
<td>.86 GB</td>
<td>.5 GB</td>
</tr>
<tr>
<td><strong>Sample Rate</strong></td>
<td>100 Msp</td>
<td>250 Msp</td>
</tr>
<tr>
<td><strong># bits</strong></td>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td><strong># Channels</strong></td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
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*+180 DSP slices (18*18 MAC)
CRC board design

- **Miniaturization of CFE Satellite Payload**
  - More capable than all CFE instrument FPGAs
  - More capable than the CFE follow-on instrument
  - Reduced lifecycle allows more relevant technology to orbit

- **Xilinx Spartan-6**
  - More power efficient than Xilinx Virtex-6
  - Very little performance loss for smaller chips
Partial Reconfiguration: “Software Defined Satellite” => Extreme Integration

I/O to Sensors, Actuators & Satellite Bus

FPGA
- Controller
- Attitude Control System
- Navigation
- SEU Manager
- System Monitor

Fixed Region
- Comms

Reprogrammable Region
- Encrypt
- Sleep

NV Memory
- Comms
- Encrypt
- MPEG
- DEMOD
- Pulse Detect
- XYZ
- Sleep

Necessary functions swapped in as needed

Upload new or refined functions after launch
Science Mission

- Measure Total Electron Content (TEC) in Ionosphere
  - Wide band RF pulse detection
  - TEC tomography using lightning strikes and generated signals
  - Test signals generated from the laboratory and transmitted to orbiting satellites
  - Joint space and ground observations are combined for generating measurements
Built-in Self-Test (BIST) development setup

Testing

- BIST can be ran without a PC, directly from the onboard computer for on orbit testing
- BIST checks CRC board for:
  - Opens
  - Shorts
  - Signal integrity
  - Memory interfaces
  - ADC interfaces
  - ADC performance
Current Status

Hardware

- Received CRC board from manufacturing 7/26/2010
- Powered on and basic functionality verified
- Further testing to be completed before full functionality is verified

Software

- GUI for BIST to verify CRC boards nearing completion
- First FPGA configuration designed to read and report ADC readings nearing completion
Challenge 1: Configuration SEUs / Device Day/ Cell

SEU as observed by CFE
Challenge 2: Power Consumption (Thermal) = f(algorithm)

- Each RCC board power usage ≈ 5 - 28W
- Each FPGA has >500 pins which are susceptible to thermal stresses
  - Maximize lifetime
    - Heat pipes limit max temperatures
    - Column Grid Array package more reliable
    - Matched CTE of thermount PCB to Ceramic Pkg
    - AlBeMet core has superior thermal transfer

without heat pipes: \( \Delta t = 50 \) deg C

with heat pipes: \( \Delta t = 17 \) deg C
Future Work

**Constellations**

- Numerous inexpensive satellites replace larger expensive satellites
- Paradigm shift allows new functions to be performed
  - Spatial separation
  - Unit replacement
- True global and persistent observation
Conclusion

- **Reconfigurable Processing**
  - Unparalleled performance
  - Extreme integration
  - Very flexible for various satellite missions and configurations
  - Upgradeable after launch
  - Serve multiple users with a single platform

- **CubeSats may allow synchronization between technology nodes and launch schedules**
  - More appropriate technology insertion schedules

- **Challenges:**
  - Need a more systematic thermal management design for high power density applications with wild swings in power consumption
  - Keep radiation tolerance and SEU management in mind
  - Small is not necessarily simple; complexity is still an issue