Understanding, Utilizing and Choosing CubeSat Kit™ PPMs

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Outline

• Part I: What is a PPM?
• Part II: Why is a particular PPM designed this way?
• Part III: Which PPM works for my CubeSat?
I: PPMs Explained

- A Pluggable Processor Module (PPM) is a small hardware module that maps a particular microcontroller (MCU) – with its unique I/O, peripherals and features – into the CubeSat Kit (CSK) architecture:
  - on the Motherboard (MB), where the radio, USB, RTC, SD Card etc. are, and …
  - on the CSK bus, the CubeSat Kit’s “backbone”
CSK Architecture Block Diagram
**PPM Connector**

The CubeSat Kit PPM connector on the PPM and the MB has I/O, power, control, status, I2C, handshaking and user signals.

The forty-eight I/O signals on the PPM are the same as those on the CSK Bus.

Eight power signals route power between the PPM and the MB.

The remaining forty signals are for control, status, I2C, handshaking, user-defined, etc.

The entire CubeSat Kit Bus connector (except for S[5..0] & MHX socket signals) is available to PPM.
PPM-to-CSK Mapping

• Dedicated / Mandatory:
  - IO.[3..0]: the first SPI interface (SPI0)
  - IO.[5..4]: the first UART interface (U0)
  - IO.[7..6]: the second UART interface (U1)
  - SCL_SYS & SDA_SYS: the first I2C interface (I2C0)
  - Control signals (e.g., –ON_SD)

• Recommended / Optional:
  - IO.[47..40]: for analog voltages AN.[7..0]
  - IO.[39..32]: for analog voltages AN.[15..8]
  - VREF0|1|2: for analog reference voltages
  - Handshake signals (e.g., HS[5..0])
II: Understanding a particular PPM

• Ideally, map any peripheral function (e.g., I/O, serial, analog) to any PPM signal.

• Generally speaking, only ASICs ($$$) and FPGAs ($) can do this. MCUs are much cheaper, and simpler to use.

• When mapping an MCU to a PPM, strive for a sensible allocation of MCU resources to the PPM signals, according to:
  ▪ Satisfy MCU-compatible power / POR / BOR / reset / programmer / debugger requirements
  ▪ Assign available peripherals to mandatory features (e.g., UARTs to U0 & U1)
  ▪ Assign available peripherals & I/O to optional features
  ▪ Assign remaining I/O intelligently to CSK Bus I/O
  ▪ Implement additional PPM features with leftover MCU resources
## PPM implementation by MCU

<table>
<thead>
<tr>
<th>PPM</th>
<th>Signals</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>I/O</td>
<td>All ports P1-P6 mapped to IO.[47..0]</td>
</tr>
<tr>
<td>MSP430F161x</td>
<td>Analog</td>
<td>VREF[2..0] utilized; AN.[7..0] on IO.[47..40] (shared w/handshaking)</td>
</tr>
<tr>
<td>64 pins (48 I/O)</td>
<td>Control</td>
<td>Shared with P1.7, P4.6, P4.5 &amp; P6.6</td>
</tr>
<tr>
<td></td>
<td>Feature</td>
<td>I2C isolator to handle I2C0-SPI0 conflicts</td>
</tr>
<tr>
<td>B1</td>
<td>I/O</td>
<td>P0-P3 mapped to IO.[29..0]; IO.[33..31] not implemented</td>
</tr>
<tr>
<td>C8051F120</td>
<td>Analog</td>
<td>VREF[2..0] utilized, AIN0.[7..0], CP[1..0] &amp; DAC[0..1] on IO.[47..34]; no VREF reference output available</td>
</tr>
<tr>
<td>100 pins (64 I/O)</td>
<td>Control</td>
<td>Via dedicated P4</td>
</tr>
<tr>
<td></td>
<td>Handshake</td>
<td>Via dedicated P5</td>
</tr>
<tr>
<td></td>
<td>Feature</td>
<td>128KB SRAM (via P4, P6 &amp; P7)</td>
</tr>
<tr>
<td>D1</td>
<td>I/O</td>
<td>48 IO ports mapped to IO.[47..0]</td>
</tr>
<tr>
<td>PIC24FJ256GAx</td>
<td>Analog</td>
<td>VREF[2,0] utilized, AN.[15..8, 7..0] on IO.[39..32, 47..40], shared w/I/O</td>
</tr>
<tr>
<td>100 pins (85 I/O)</td>
<td>Control</td>
<td>Via dedicated I/O</td>
</tr>
<tr>
<td></td>
<td>Handshake</td>
<td>Via dedicated I/O</td>
</tr>
<tr>
<td></td>
<td>Feature</td>
<td>64Mbit serial Flash memory, U2, U3, SPI1, SPI2, I2C1 &amp; I2C2 free and mapped to CSK Bus</td>
</tr>
</tbody>
</table>
PPM A/B/D Commonality

• Get power from +5V_SYS and/or +5V_USB
• Provide VCC & VCC_SD @ +3.3V
• External Reset / POR / BOR circuit
• External OFF_VCC input
• External SENSE and -FAULT_OC outputs
• USER[11..0] untouched
III: The Right PPM for the Job

• Is the MCU compatible with your code?
• Does the MCU have the features / speed / power you want / need?
• Will shared signals work in your design?
• Do you like the compatible tools (e.g., IDEs, compilers, debuggers)?

• MCU migration is usually within families, so invest in a MCU architecture wisely.
Conclusion

• Purely in terms of I/O and CSK standard peripherals (i.e., SPI0, U0, U1 & I2C0), PPMs are nearly interchangeable from a hardware perspective.

• MCU-specific differences are reflected in functions of signals IO.[47..8], and MCU internal capabilities.

• Dedicated control & handshaking is better than sharing I/O pins, but requires more than 48 I/O pins.

• Surplus pins are used on-board PPM to implement additional general-purpose features attractive to all CSK customers.

• Mission-specific features should be implemented through the MCU’s I/O space via the CSK Bus.
Q&A Session

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and:

Appendix

• Speaker information
  - Dr. Kalman is Pumpkin's president and chief technology architect. He entered the embedded programming world in the mid-1980's. After co-founding Euphonix, Inc – the pioneering Silicon Valley high-tech pro-audio company – he founded Pumpkin, Inc. to explore the feasibility of applying high-level programming paradigms to severely memory-constrained embedded architectures. He is the creator of the Salvo RTOS and the CubeSat Kit. He holds two United States patents. He is a consulting professor in the Department of Aeronautics & Astronautics at Stanford University and directs the department’s Space Systems Development Laboratory (SSDL). Contact Dr. Kalman at aek@pumpkininc.com.

• Acknowledgements
  - Pumpkin's Salvo and CubeSat Kit customers, whose real-world experience with our products helps us improve and innovate.

• CubeSat Kit information
  - More information on Pumpkin's CubeSat Kit can be found at http://www.cubesatkit.com/.

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