

# Electronics systems design on CP2



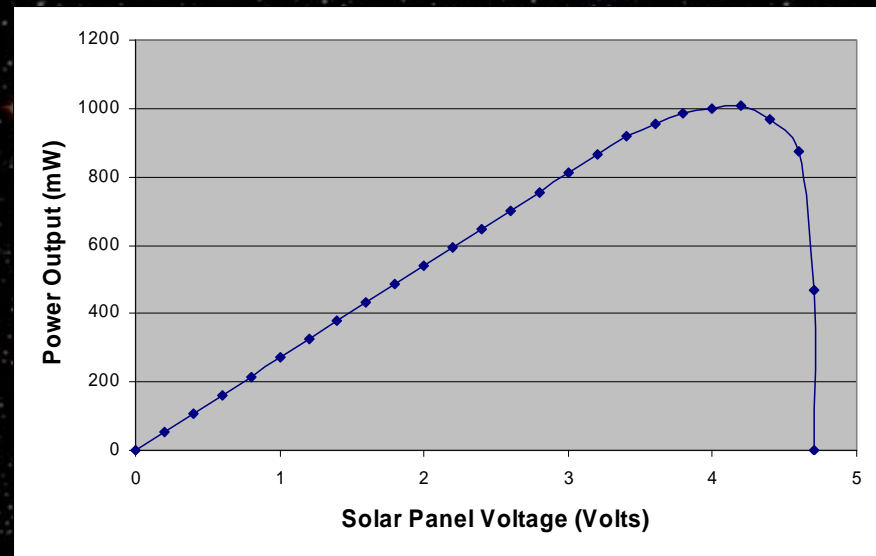
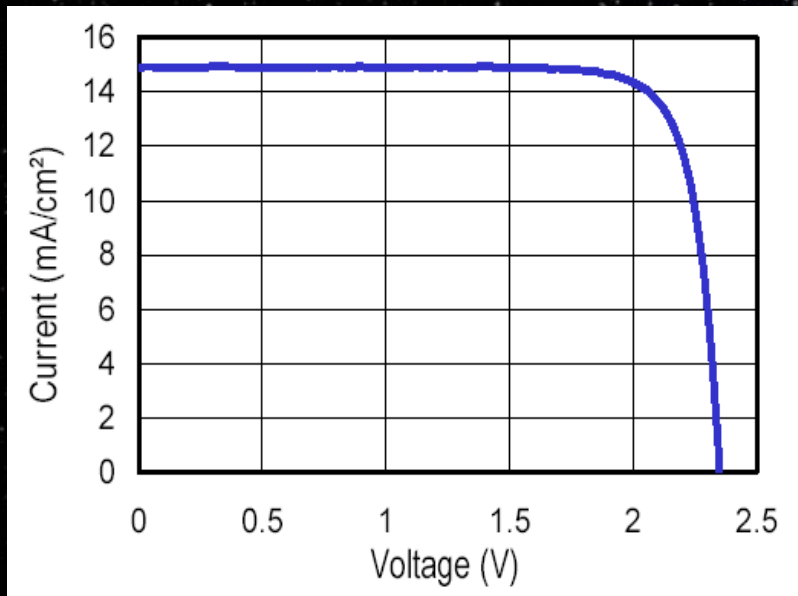
# Electronics systems design on CP2

## CP2 Innovations:

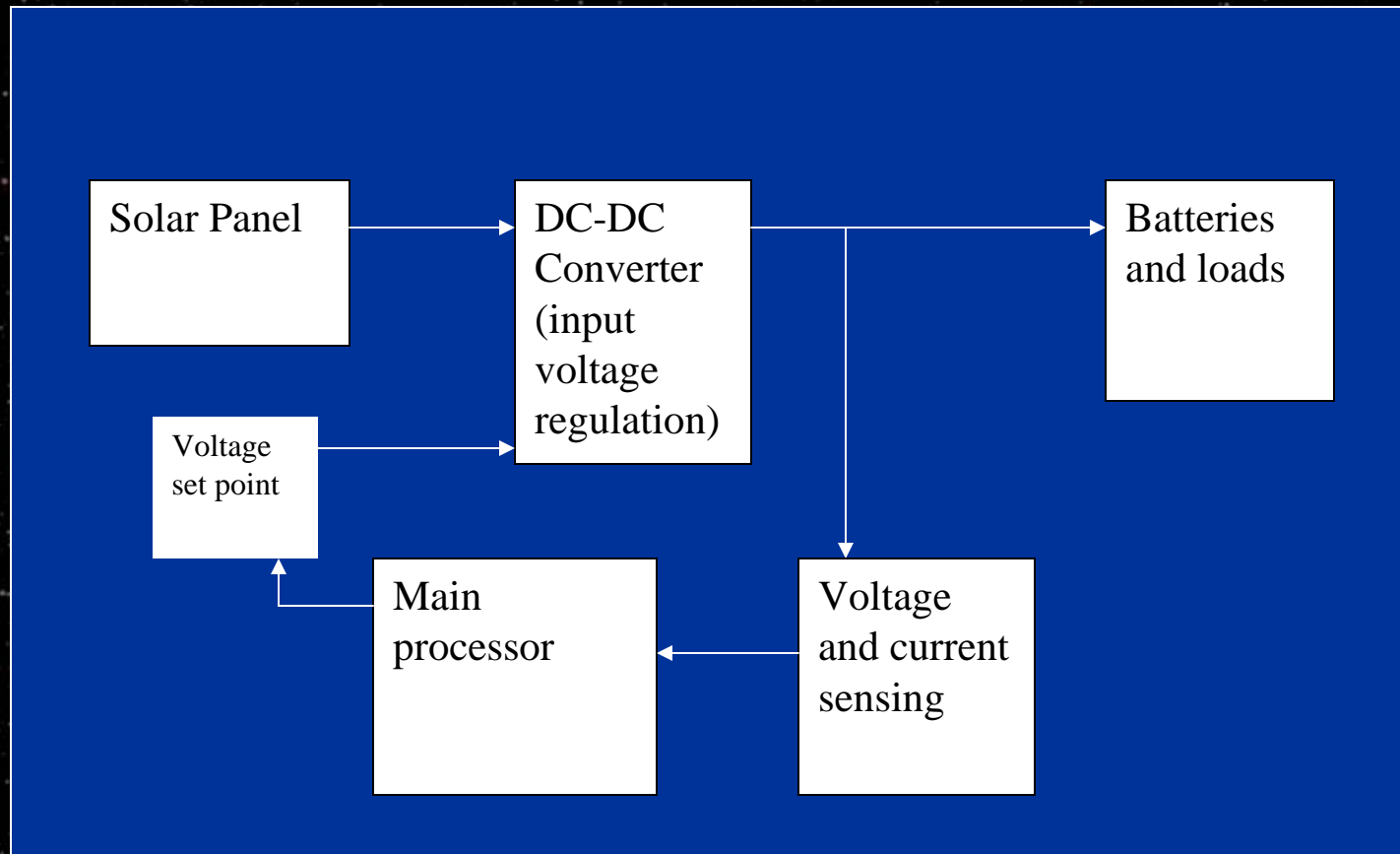
- Software TNC
- Redundant Communication Systems
- Maximum Power Point Tracking
- Power Distribution Failure Isolation
- Robust I<sup>2</sup>C Architecture

# Maximum Power Point Tracking

- Solar Panel Characteristics
  - GaAs Dual Junction, 21.5% eff. From Spectrolab



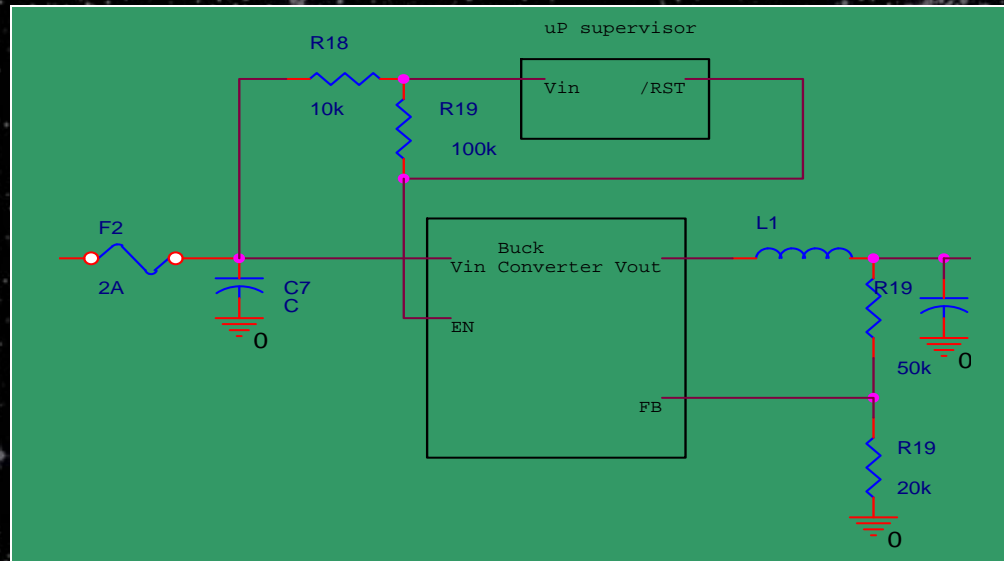
# Maximum Power Point Tracking





# Load Power Conditioning

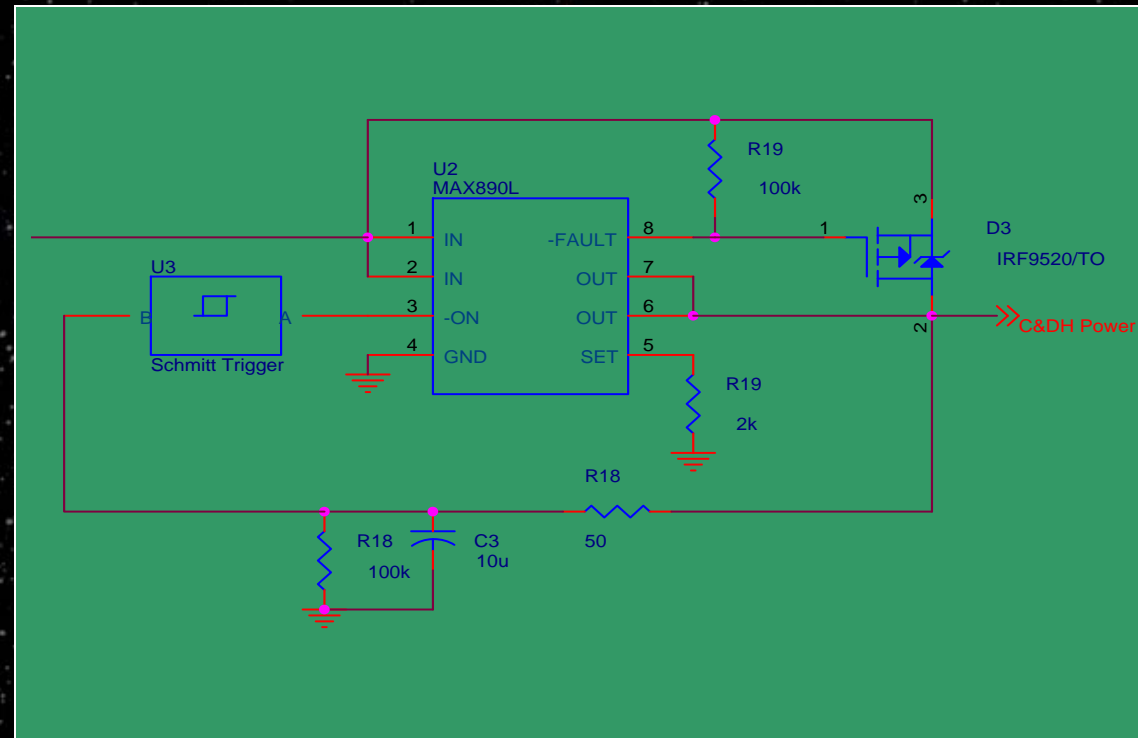
- Under-Voltage Shutoff (with hysteresis)
  - Uses a uP Supervisor IC
  - Low voltage set point set by uP Supervisor
  - Hysteresis set by resistors that reduce voltage “seen” by the uP Supervisor



# Load Power Conditioning

- Smart fuse

- Designed around the MAX890L
- Limits current flow to the load devices
- Shuts off power if current flow reaches limit for a given period of time
- Re-enables power for a brief period to test for continued fault condition



# Energy Storage

- Li-ion vs. Ni-Mh
  - Energy density
  - Space Shuttle requirements
- For maximum power density and Space Shuttle compatibility, CP2 will be able to accommodate both types of batteries
- For redundancy, 2 batteries and battery protection circuits will be used



# Energy Storage

- Batteries selected:
  - Li-ion: PolyStor Corp. 3.7V, 1200mAh
  - Ni-Mh: GP Batteries, 3.6V, 700mAh

Li-ion



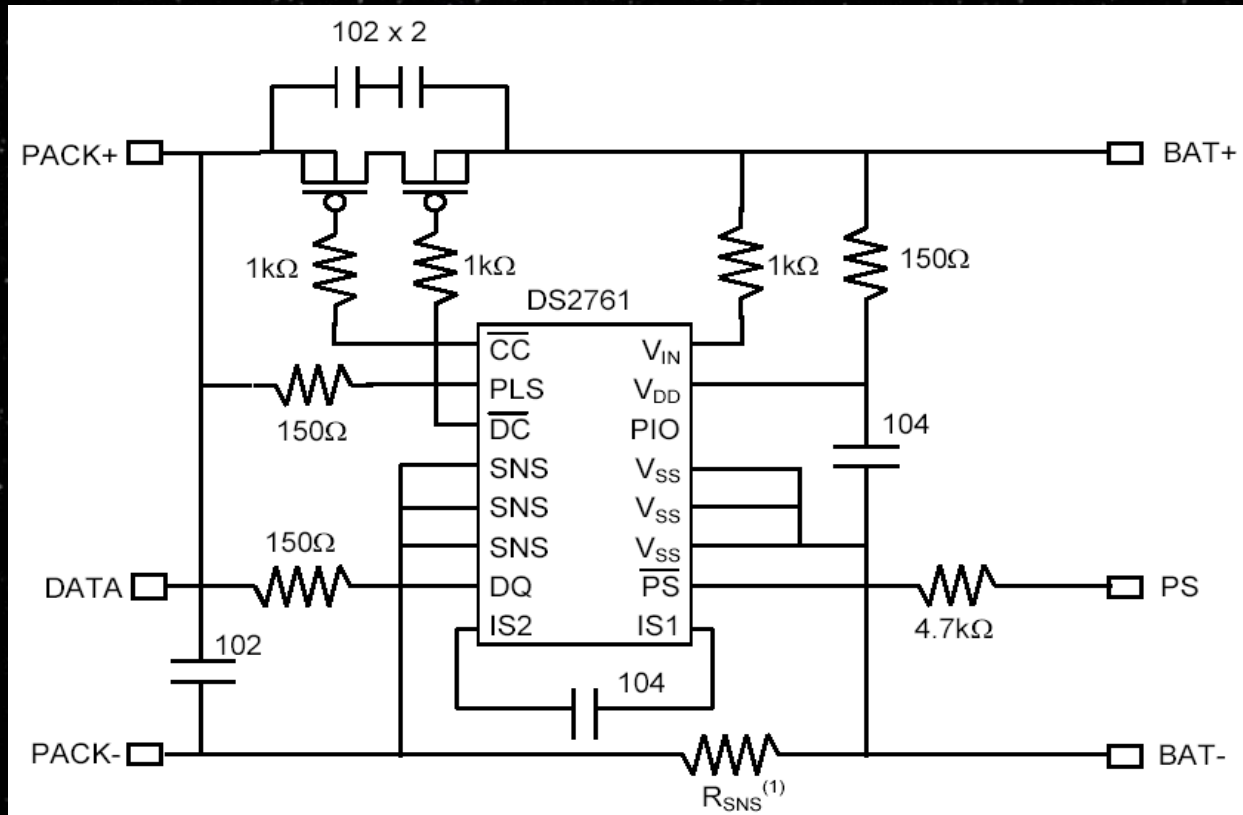
Ni-Mh





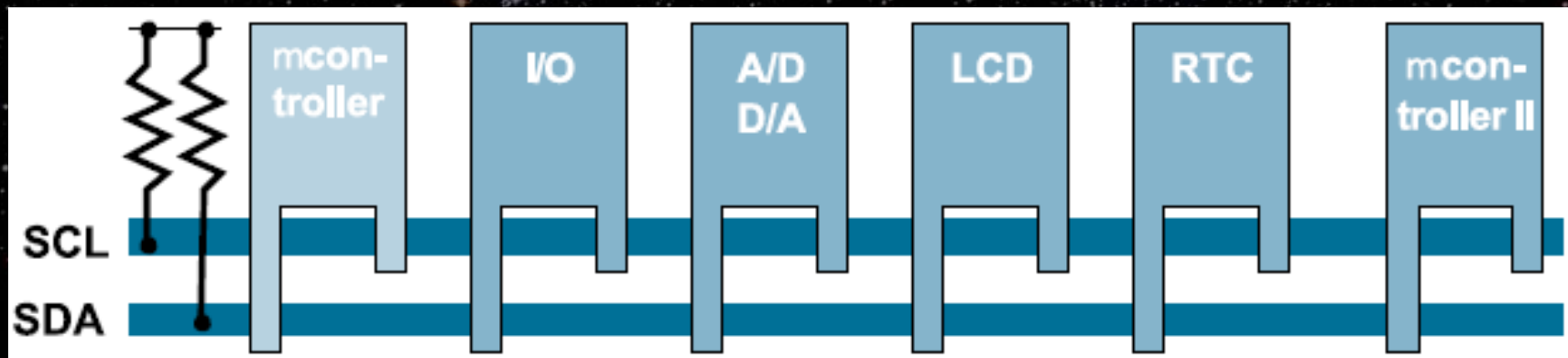
# Energy Storage

- Battery monitor and protection circuitry



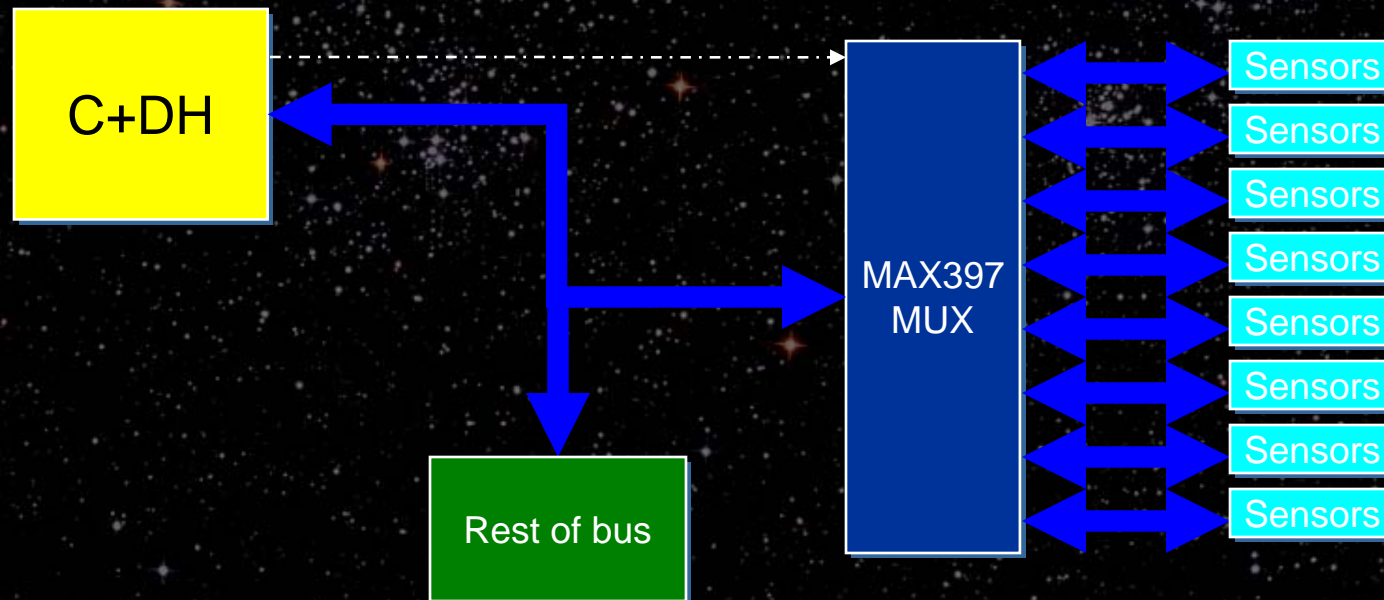
# I<sup>2</sup>C Protocol

- Only 2 wires required
- Many devices use it
- Multiple masters can use the bus
- Address limitations
- Single point failure!!!!!!



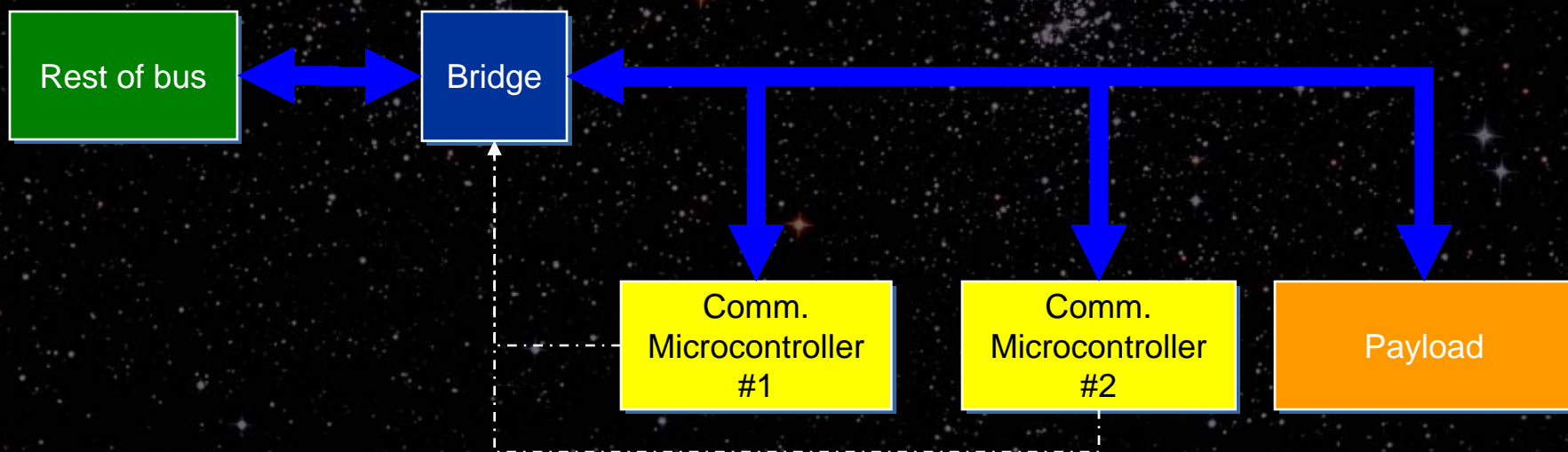
# I<sup>2</sup>C MUX system

- Allows selection between 8 I<sup>2</sup>C bus branches
- Each side of CP2 is given a different branch
- Prevents failure on any branch from crippling entire system
- Several devices with the same I<sup>2</sup>C address can be used



# I<sup>2</sup>C Bridge and Contingency Mode

- Enabled in the event of a main bus or C+DH processor failure
- Isolates all but the communications system and the payload for minimal functionality





# Design Questions?

