

Development of Two High-Energy Bus 'Cores'

FOR RAPID SUPPORT OF LOW-TRL AND EDUCATIONAL PAYLOADS

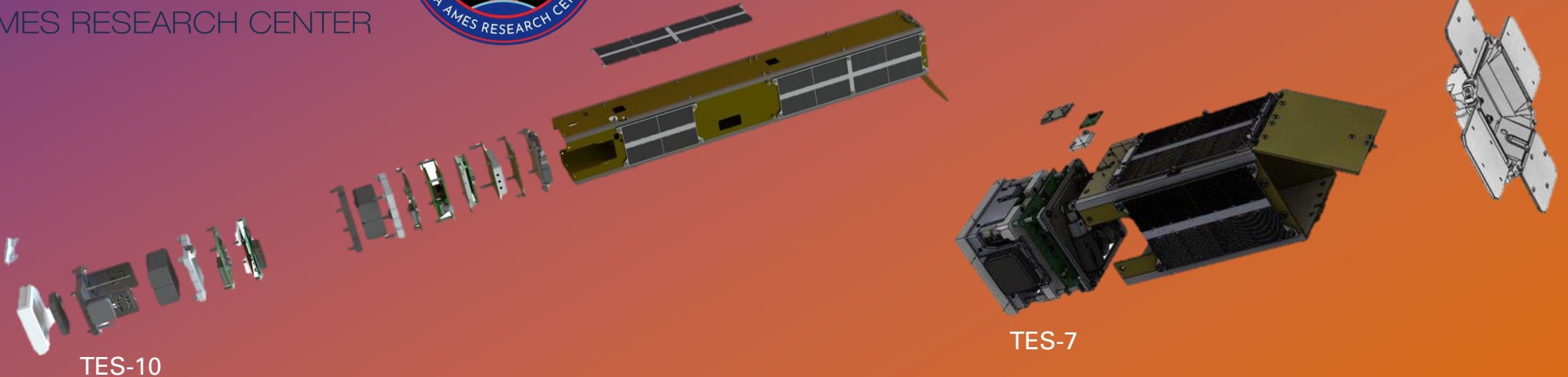
now The Nano Orbital Workshop

Rapid Flight Development Group



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AMES RESEARCH CENTER



TES-10

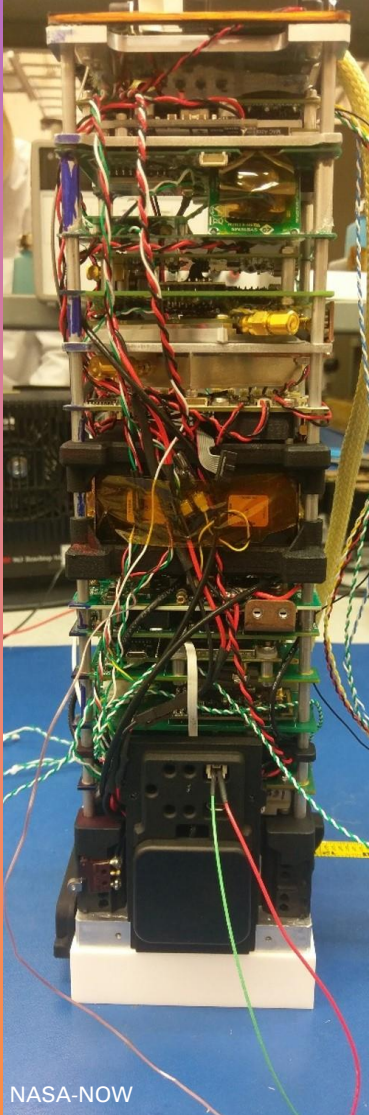
TES-7

+ ● Avery Brock, EE
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DEVELOPMENT OF TWO HIGH-
ENERGY BUS CORES



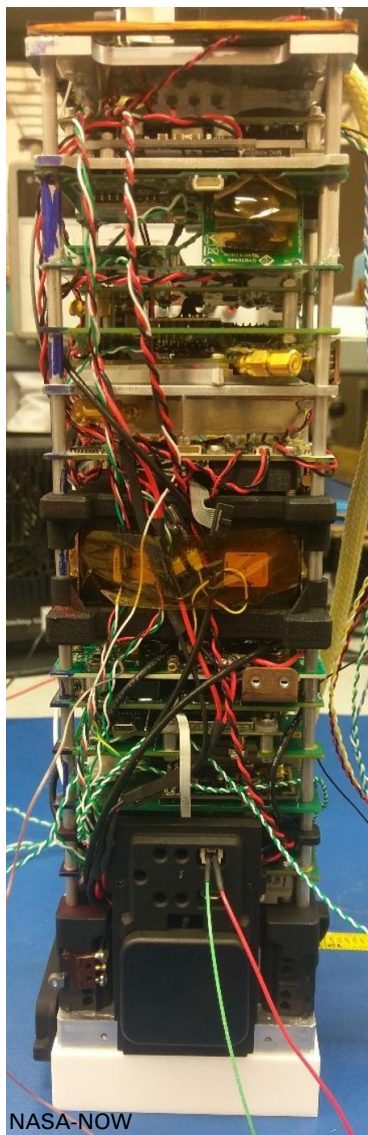
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OUTLINE

TechEdSat Heritage Design
The Challenge of Flexibility
Spacecraft CoreStack Concept

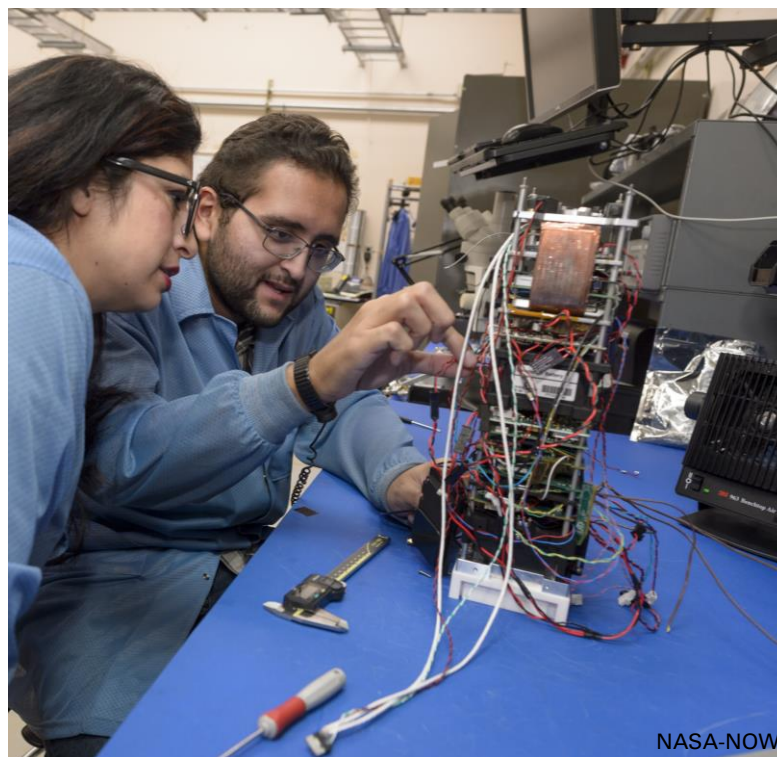


TechEdSat Stack Architecture:

- PC/104 perimeter PCBs, non-standard interconnects
- Discrete sub-systems are stacked and wired together

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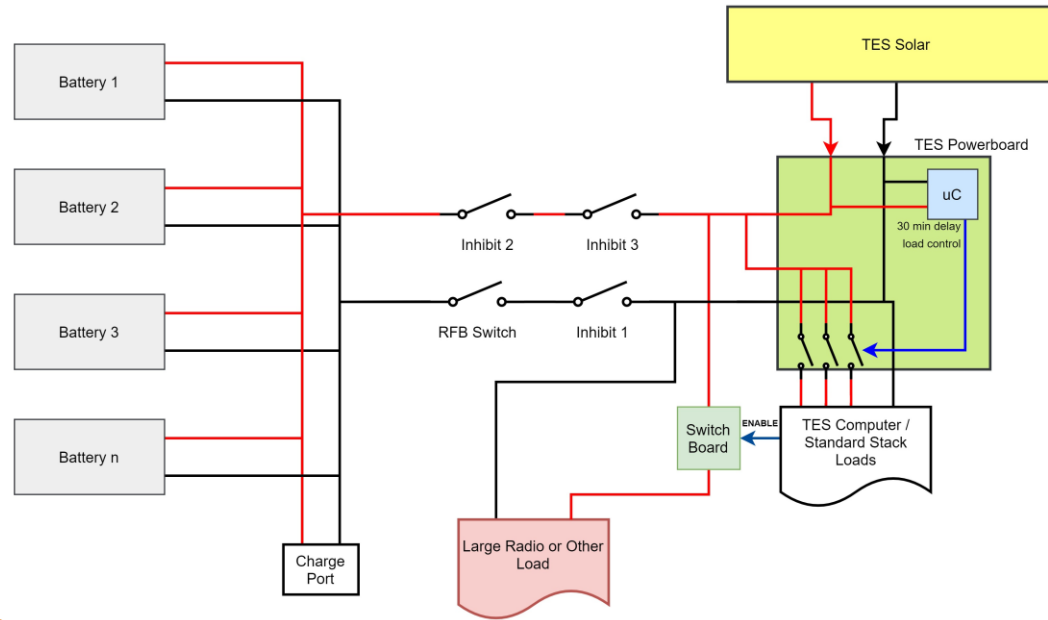
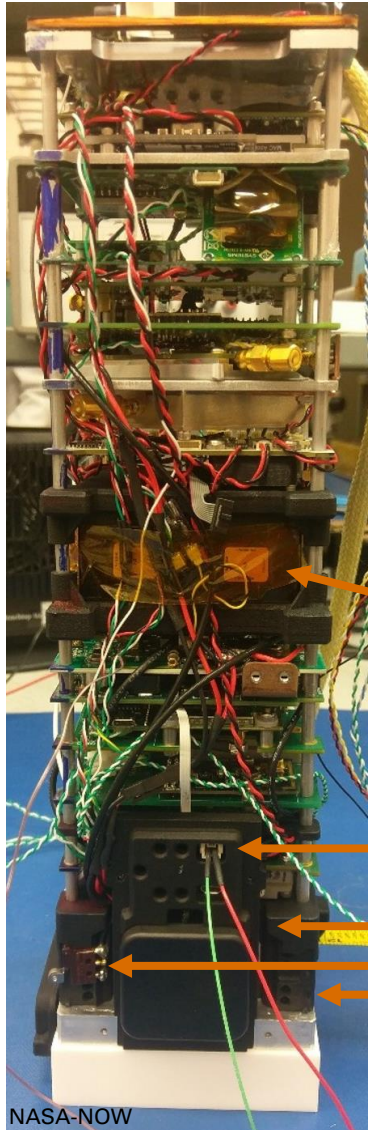


Benefits:

- Very open standard provides extreme payload flexibility
- Makes design of and integration with structure easy

Drawbacks:

- Hand-wiring of system is complex and time consuming
- Difficult to debug harnessing is sub-optimal



Battery Pack Set B

Charge Port

Battery Pack Set A

Mechanical Inhibits

Inhibiting:

- ISS PSRP-approved inhibit scheme using triple-redundant mechanical switches
- 15-to-30-minute activation delay for radios, instant-on or software delay for payloads and other systems

Power Management:

- Direct connection of batteries to PDS and solar arrays (panel-based MPPT)
- ISS-approved COTS camera batteries have built-in protections and charge limiting
- Six-inch spacing requirement between 10Ah packs per ISS PSRP

Design has functioned for 20+ missions, but TES is outgrowing its power architecture

'Tardigrade' All-In-One Solution (Second-Gen)



40-Watt All-In-One Board

- **Vorago VA10820 processor**
 - 128KB flash, 32KB RAM
 - 50 MHz ARM Cortex-M0 32 bit
 - Rad-Hardened
 - **Six 2A solar panel channels**
 - Channel power monitoring
 - **Single battery channel**
 - Power monitoring
- External load buck or boost supplies and motor drivers
 - Iridium 9603 and 2.4 GHz XBee3
 - Mini GPS, Thermocouple channels, and a 3-axis Magnetometer

A single-board satellite design that was not pursued and fully developed; not quite the right fit

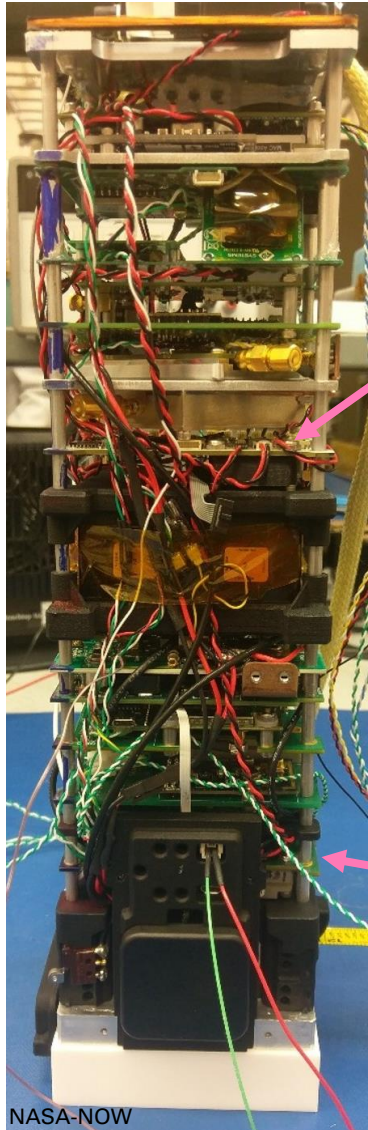
'Powerboard' Core C&DH and Power (First-Gen)



14-Watt Power and Communication Board

- **ATmega328 processor - obsolete**
 - 32KB flash, 2KB SRAM
 - 16 MHz 8-bit processor
- Half the memory of Apollo Guidance, yet running full missions with two bytes of free memory**
- Four 3A solar panel channels
 - Channel voltage monitoring
 - Single battery channel
 - Voltage and discharge current monitoring
 - Power supply outputs to subsystems and driver for Exo-brake deployment
 - Iridium 9602 modem

6U TES-10



NASA-NOW



NASA-NOW

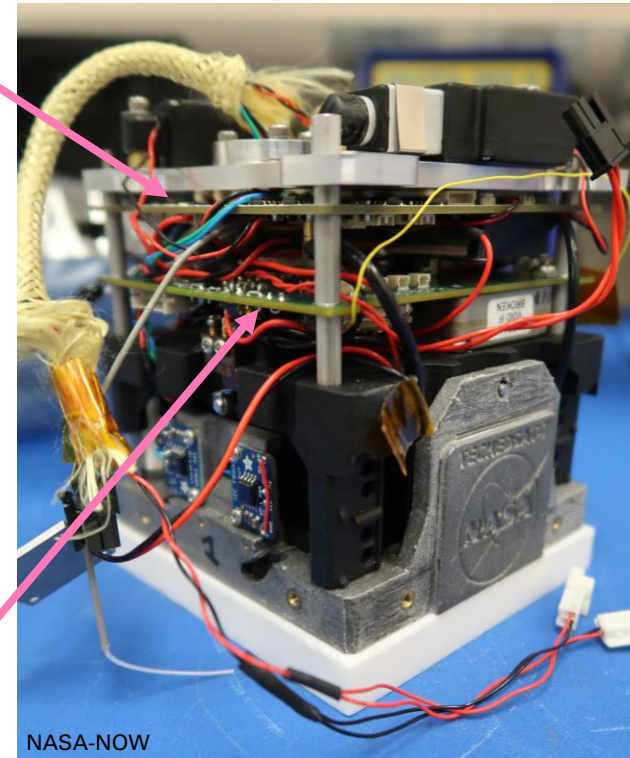
'Tardigrade' All-In-One
Solution (Second-Gen)

'Powerboard' Core
C&DH and Power
(First-Gen)



NASA-NOW

2U TES-7



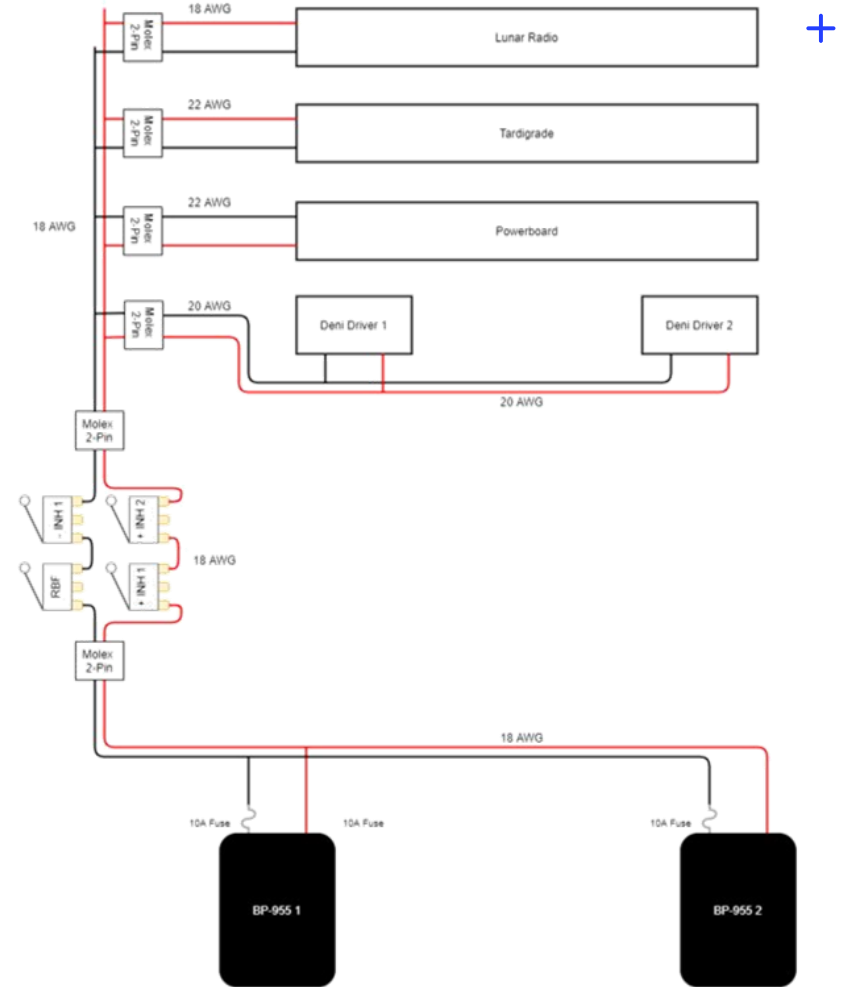
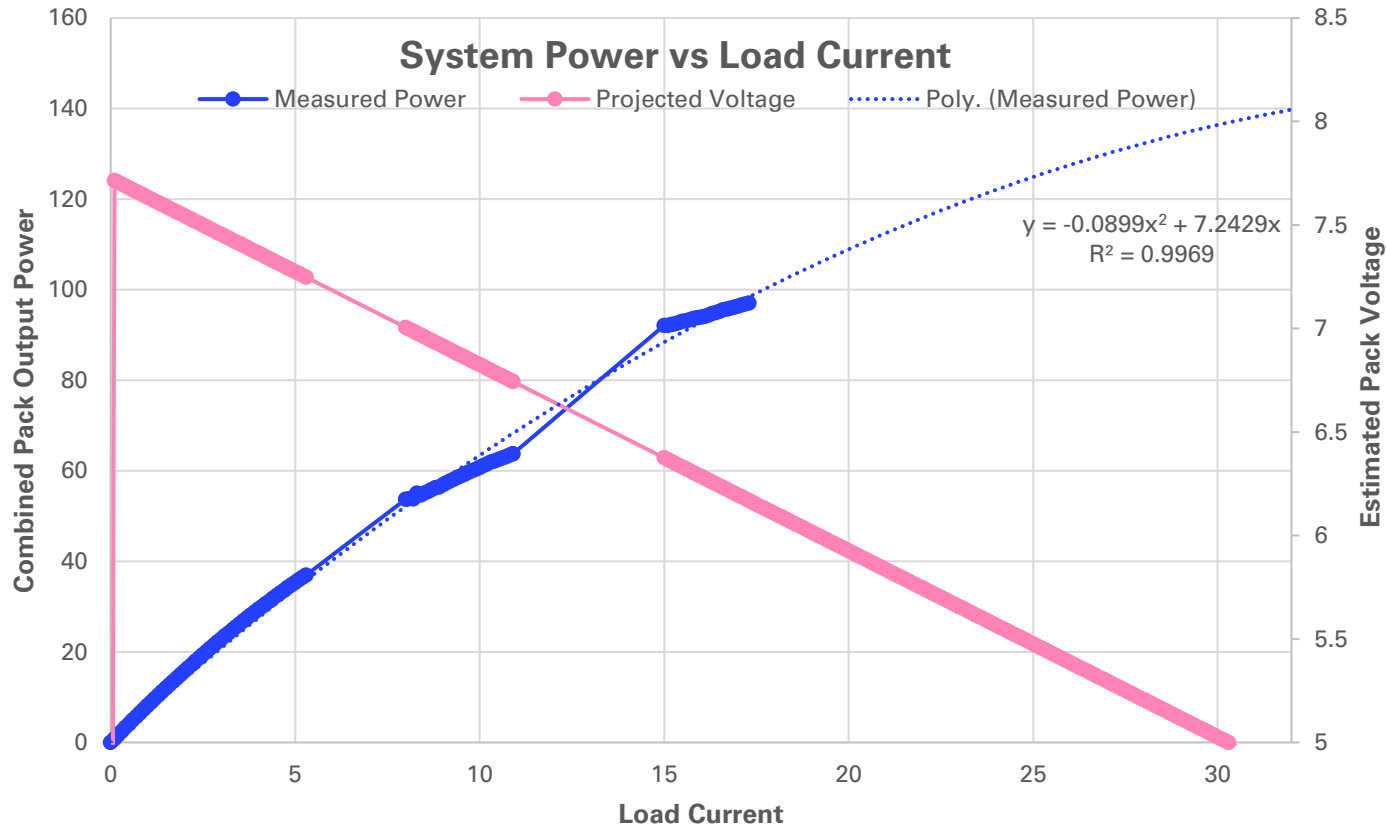
NASA-NOW

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**Combined C&DH and
EPS/EPD single-board
modules, i.e.
Spacecraft 'Cores'**

**Powerboard has been
the backbone of every
TES mission, with
Tardigrade recently
supplementing**

Single low-voltage feed via mechanical inhibits inherently limits total system power due to resistive losses, regardless of Core design

Existing Cores cannot support a 50W payload

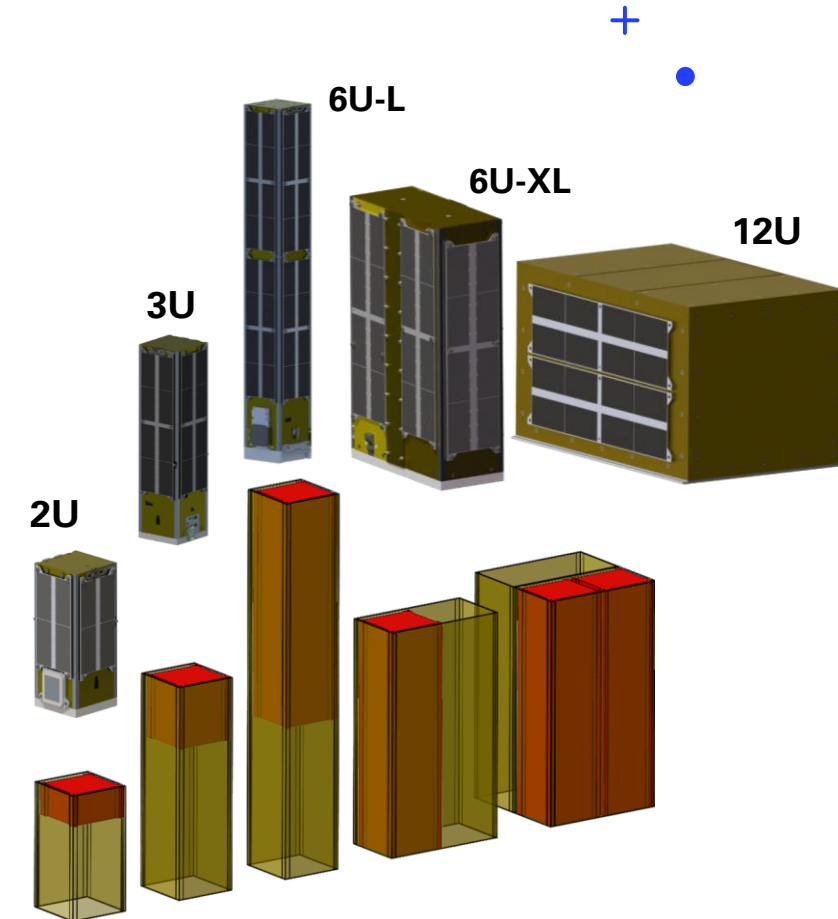


1. Support a multitude of bus sizes and power capabilities with a minimum of hardware:

- 0.5U, 1U, 3U, 6U-L, 6U-XL, & 12U+ Bus Sizes
- 10, 20, 30, & 40Ah+ battery pack configurations
- Balloon, sub-orbital, orbital, ISS, and beyond LEO mission desires

2. Support ISS PSRP heritage compliance while also supporting new space launchers and high-energy systems

3. Explicitly support third-party ‘black-box’ payloads, i.e., provide clean standardized interfaces unused by core avionics



NOW bus sizes with expected payload volume in red



TES 'Mini-Sat' Configuration: Minimum Bus 10Ah 50W Power Budget

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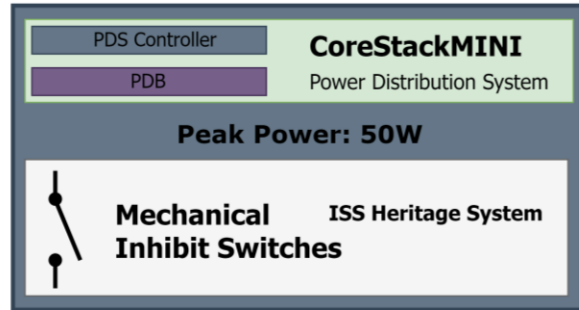


Battery Packs

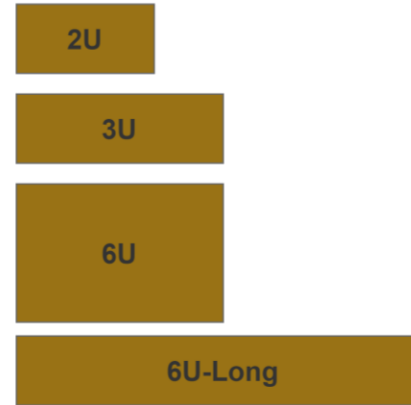


Capacity: 10Ah, 50W

Core Options



Bus Size



Solar Capacity

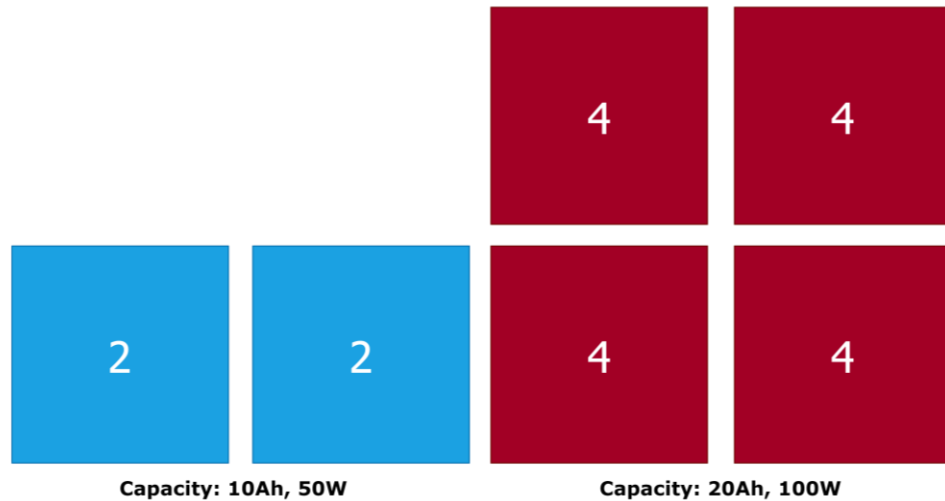


50W ISS Heritage System – Direct Replacement

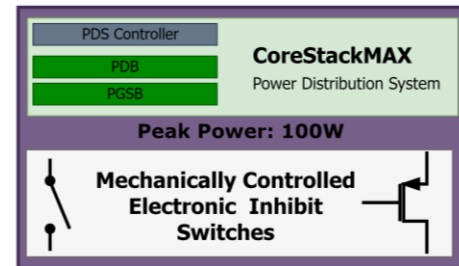
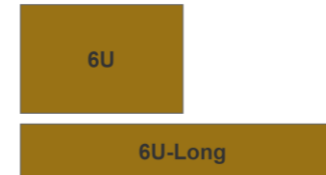
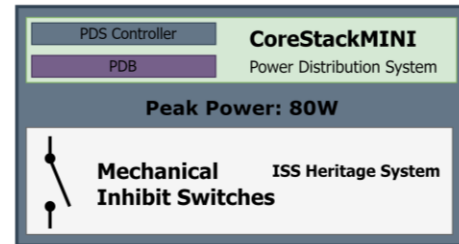
Solar Assumes TES SoA: 3.67 W/sqU, 3 sqU and endcaps uncovered

TES 'Standard' Configuration

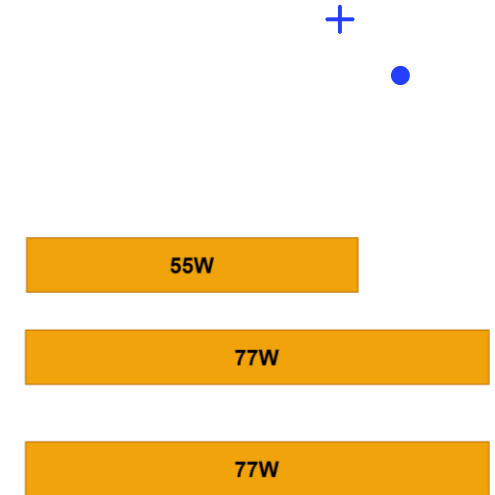
20Ah 80W ISS Power Budget
20Ah 100W New-Space Power Budget



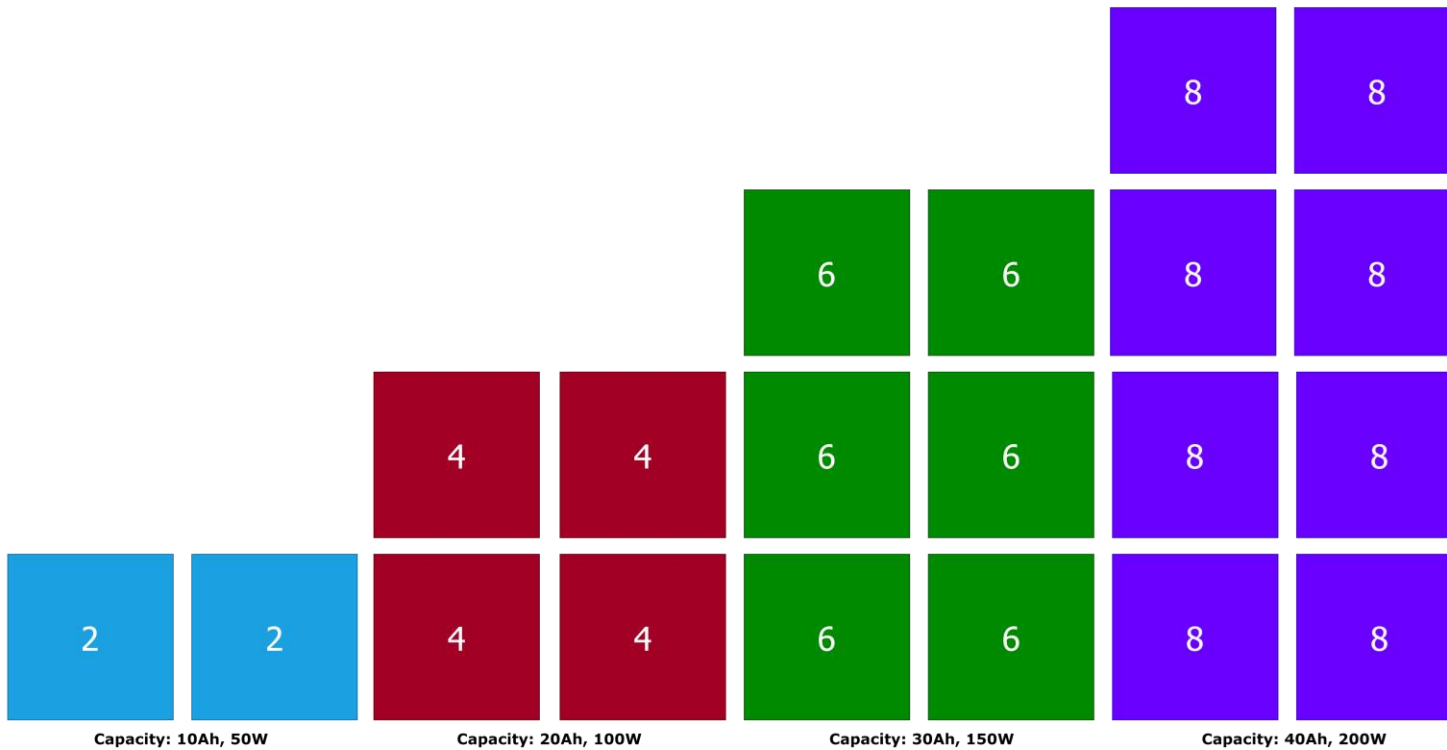
CoreStackMINI: 80W ISS Heritage System – Upgrade



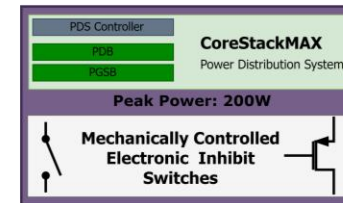
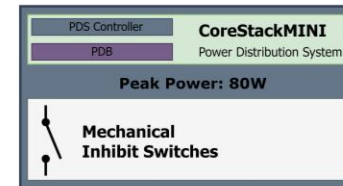
CoreStackMAX: 100W System – Novel Hardware



TES 12U Configurations Up to 40Ah 200W Power Budget on New-Space Launchers

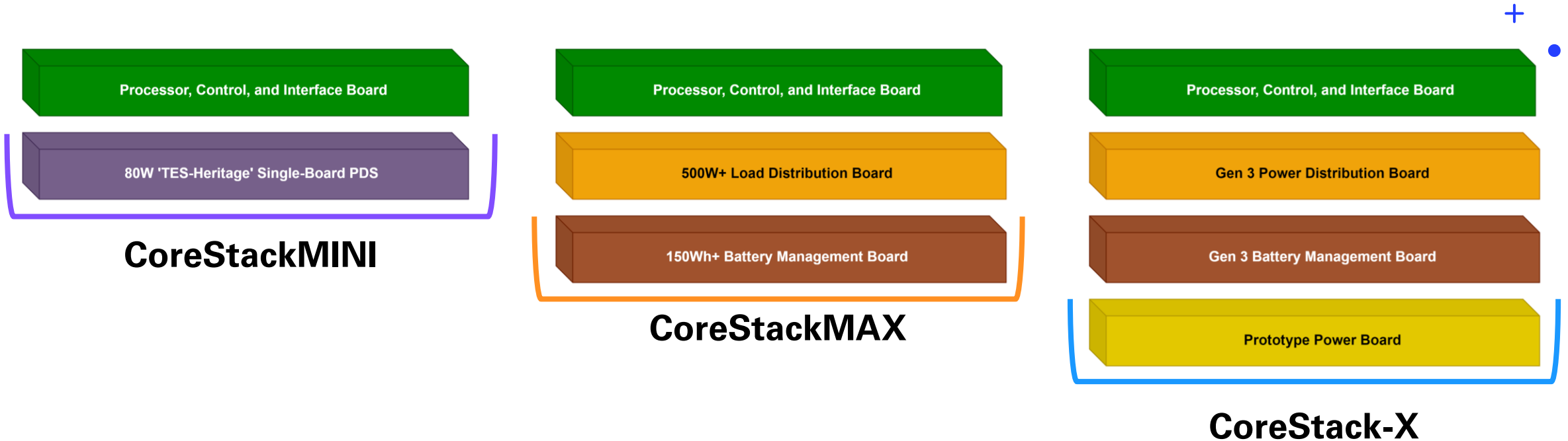


CoreStackMINI: 80W ISS Heritage System – Upgrade



CoreStackMAX: 200W System – Novel Hardware

Create a minimum set of hardware to support all configuration options



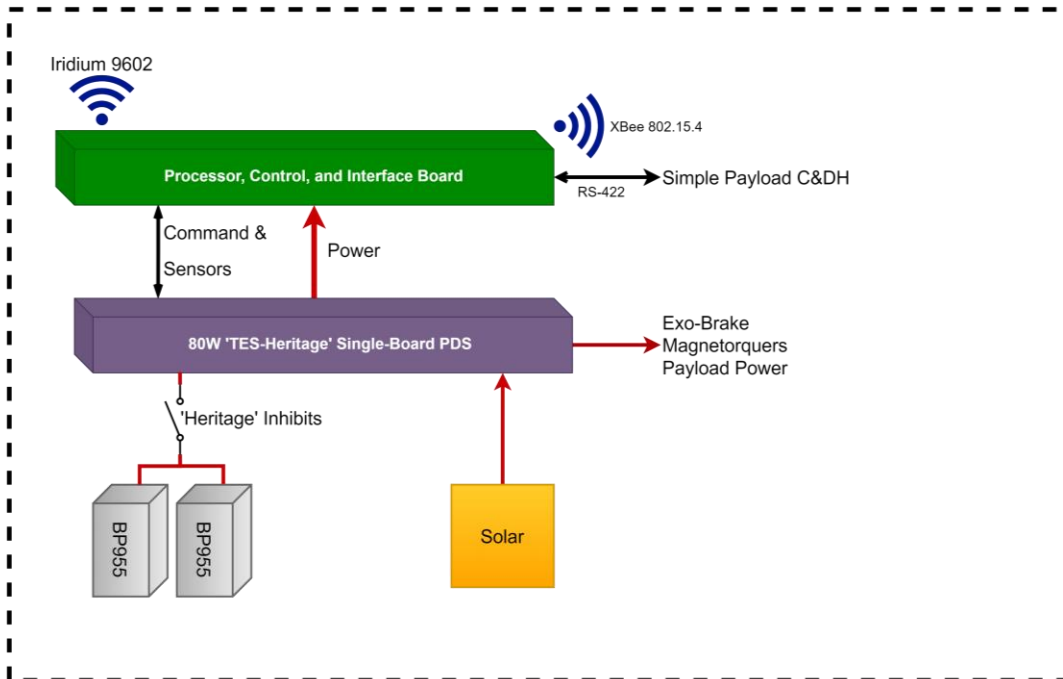
One Controller board to standardize processor, code, and comms

Two sets of Power Distribution/Management boards designed to two broad power and inhibit schemes

Satellite Configurations:

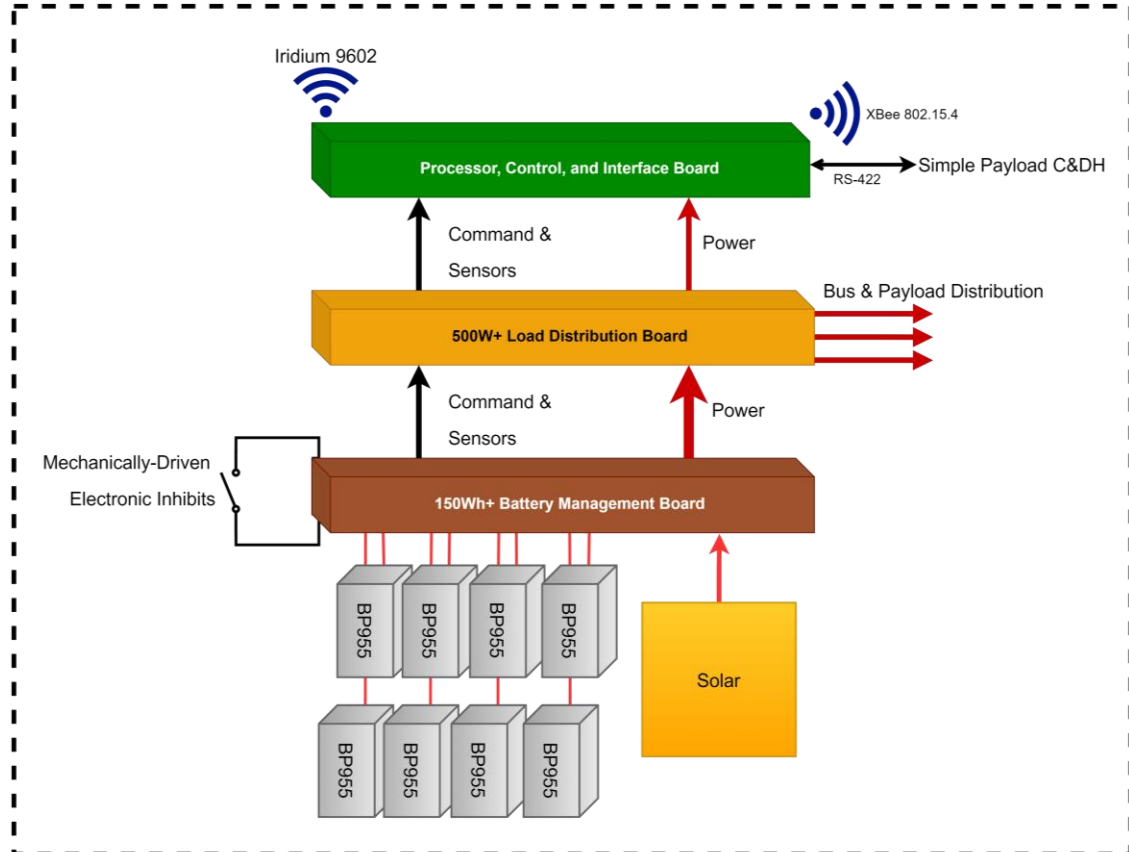
Minimum Bus

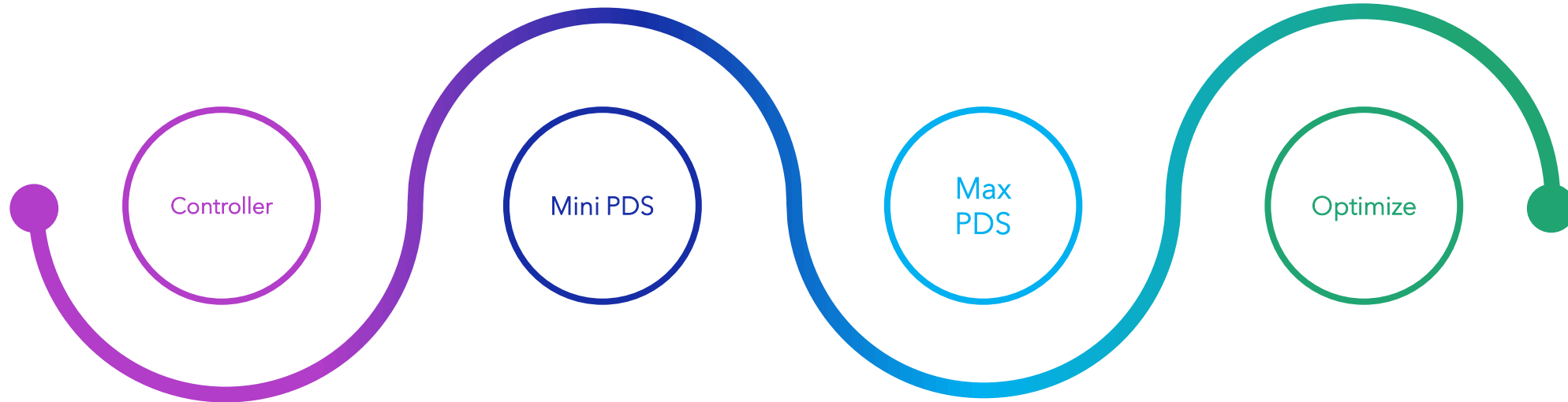
CoreStackMini with single-board mini-power system



Maximum Bus

CoreStackMAX with dual-board PDS





Controller

Complete the design and layout of new CoreStack controller; start software development

Mini PDS

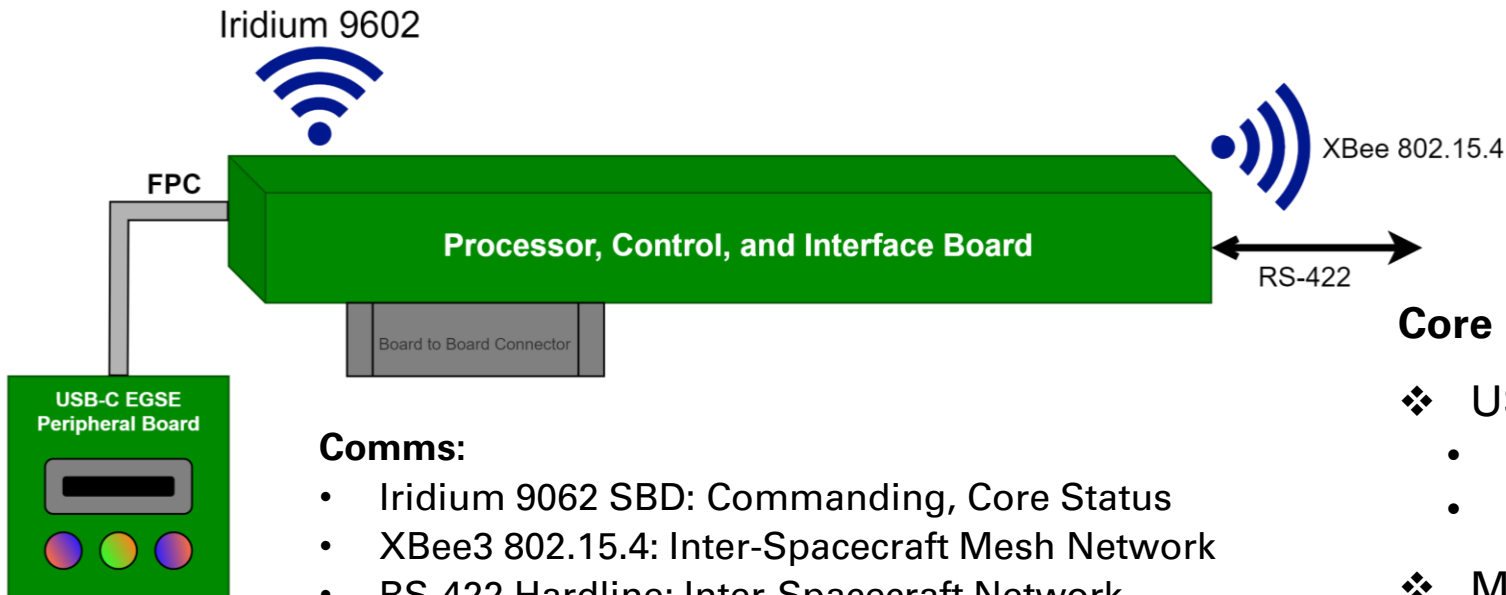
Complete the design of and build the new single-board ISS-inhibit scheme 80W PDS and fly it

Max PDS

Develop the two-board 200W+ PDS stack and begin laboratory and environmental testing

Optimize System

Begin optimizing other TES systems to better mesh with the new CoreStack system to ease integration



Comms:

- Iridium 9062 SBD: Commanding, Core Status
- XBee3 802.15.4: Inter-Spacecraft Mesh Network
- RS-422 Hardline: Inter-Spacecraft Network

Memory:

- 8Mb Program FRAM – Vorago MCU
- 4Mb Data/Configuration FRAM

Other:

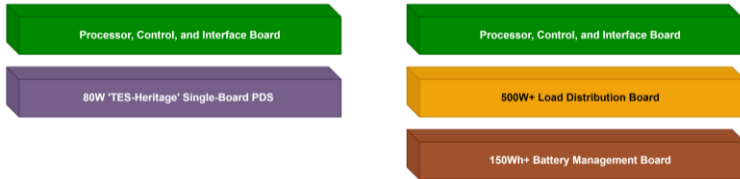
- Flight-Heritage RTC
- GPS Signal Feedthrough
- Standardized Board to Board Interface
 - Unconstrained serial interfaces, no GPIO limitations

Core Features:

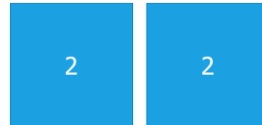
- ❖ USB-C Single-Point EGSE
 - 60W USB-C PD-Compliant Charging
 - Status LEDs and USB 2.0 Link
- ❖ Multiple Processor Options
 - Interoperable footprints for several microcontrollers
 - Teensy 4.0, 3.2 – TES Heritage
 - Adafruit Feather – SAMD21 ARM-M0, SAMD51 ARM-M4
 - Embedded Vorago ARM-M4 Rad-hard
- ❖ Single-Board Blackbox
 - Total power system failure survival with sensor polling and final packets comms



Four new pieces of hardware:



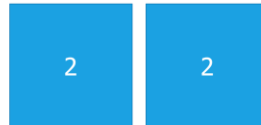
Battery Packs



Capacity: 10Ah, 50W



Capacity: 20Ah, 100W



Capacity: 10Ah, 50W



Capacity: 20Ah, 100W



Capacity: 40Ah, 200W



Capacity: 30Ah, 150W

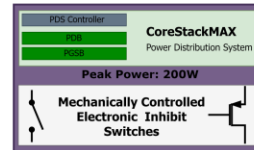
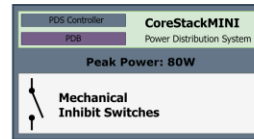
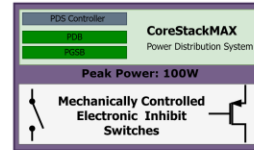
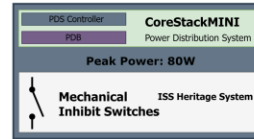
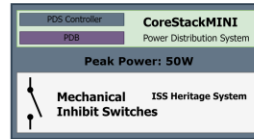


Capacity: 20Ah, 100W

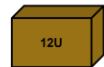
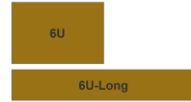
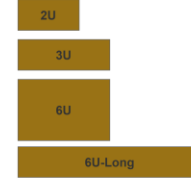


Capacity: 10Ah, 50W

Core Options



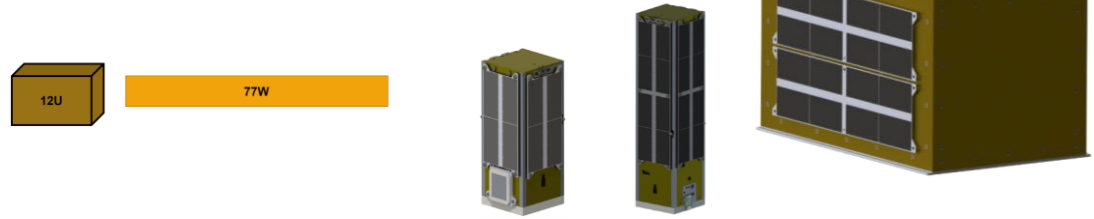
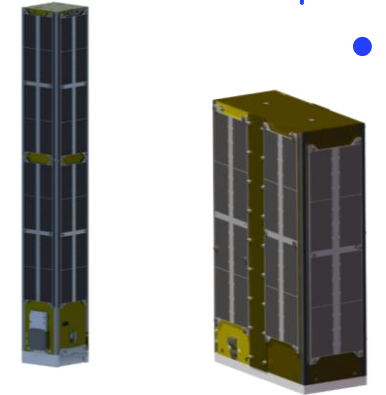
Bus Size

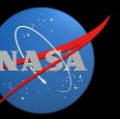


Solar Capacity



Yields **14** bus configurations to meet ANY launch opportunity





Development of Two High-Energy Bus 'Cores'

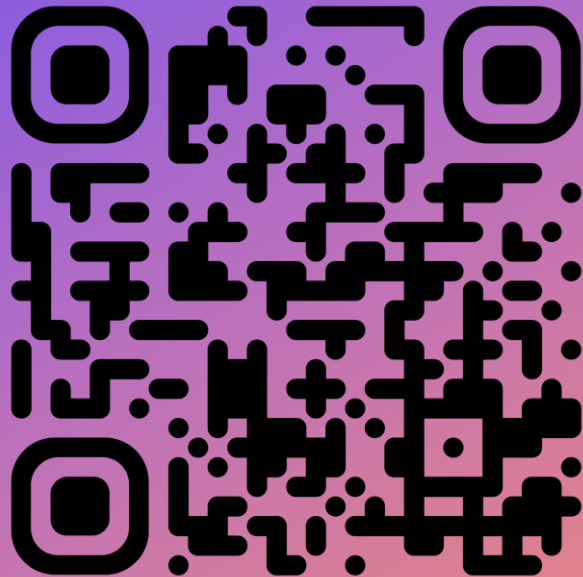
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